SECTION 5 MAINTENANCE

5.1 INTRODUCTION.

5.2 This section contains maintenance information for the counter. Included are TTL theory, ECL theory, diode gate theory, signal flow in all modes of operation, troubleshooting, and diagrams to localize, isolate and locate defective components. Performance check procedures are not included in this section, but can be found in Section 3.

5.3 RECOMMENDED TEST EQUIPMENT.

5.4 Test equipment recommended for maintaining, troubleshooting, and servicing the counter is listed in table 5.1. Test equipment with equivalent characteristics may be substituted for equipment listed.

5.5 CALIBRATION.

5.6 Internal Reference Oscillator Adjustment.

5.7 The following procedures are given for adjustment of the counter's internal reference oscillator. One of three different reference oscillators may be used in the counter. The reference oscillators are as follows:

a. Standard Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730551

b. Option 050 Temperature-Compensated Crystal Oscillator (TCXO); Dana part number 730578

c. Option 200 Temperature-Compensated Reference Oscillator (TCRO); Dana part number 730228

5.8 For standard and option 050 reference oscillators, perform the following set-up procedures.

a. Set the counter controls as follows:

Control	Setting
DISPLAY TIME	about 9 o'clock
FUNCTION	FREQ A
TIMEBASE	10 second
A Slope	Plus (+)
A Coupling	DC
A Trigger Level	PRESET
SEP/COM	SEP
STORAGE	ON
REF	INT OUT
A Input Voltage Range	10

Table 5.1 - Required Equipment

Instrument Type	Required Specification	Recommended Instruments
Frequency Standard	1 MHz, 5 MHz, or 10 MHz	
Oscilloscope	150 MHz Bandwidth 500 MHz Bandwidth	TEK 454 TEK 7900
Voltmeter	10 mVDC to 200 VDC	Dana 4300
Sine Wave Generator	2 Hz – 10 MHz	Dana 7010
VHF Signal Generator	10 – 150 MHz	HP8654A
VHF Signal Generator	1 – 550 MHz (Not required for 8010B)	HP8654A
Pulse Generator	4 ns pulsewidth	Datapulse 112
Alignment Tool	.075" Hex (nonmetallic)	General Cement 9300
Alignment Tool	Blade (nonmetallic)	
Sampling Voltmeter	0 – 600 MHz	HP3406
BNC "T" connector		
50Ω Tee connector		HP 10221A
2 – BNC to GR Adaptors		

b. Connect a 1 MHz frequency standard to A input.

c. Allow 1 hour time for the counter temperature to stabilize.

d. The difference between the internal reference oscillator and the 1 MHz frequency standard can be determined by the following formula:

Internal Oscillator Frequency = (20,000,000 – Counter Reading). See table 5.2.

Table 5.2 - Reference Oscillator Error

Counter Display	Internal Reference Osc.
999.9950 kHz	10000.050 kHz
999.9975 kHz	10000.025 kHz
1000.0000 kHz	10000.000 kHz
1000.0025 kHz	9999.975 kHz
1000.0050 kHz	9999.950 kHz

5.9 ADJUSTMENT PROCEDURE – STANDARD TCXO.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

a. Apply power to the counter for one hour before attempting TCXO adjustment (see paragraph 5.8). Remove the top cover (see paragraph 5.18, "Access to P.C. Boards"). Locate the TCXO located on the Readout assembly near the rear of the counter (see figure 6.5, Readout Layout). Remove the #6 metal or nylon cap screw on the top of the reference oscillator. Use a nonmetallic alignment tool for adjustment. Some oscillators require a hexagon .075 dia. alignment tool, and others require a blade type.

b. Insert the proper adjustment tool into the #6 screw hole on the top of the reference oscillator. Adjust the TCXO until the display reads 1000.0000 kHz. Wait ten seconds and readjust the TCXO if the first adjustment was not correct. Remove the adjustment tool.

c. After the initial adjustment, replace the cap screw and the top cover. Allow 30 minutes for temperature stabilization and recheck the reading.

5.10 ADJUSTMENT PROCEDURE – OPTION 050 TCXO.

5.11 Allow the counter to temperature stabilize for one hour before adjustment and verify one hour after adjustment. Follow the procedures outlined in paragraph 5.9.

5.12 ADJUSTMENT PROCEDURE – OPTION 200 TCRO.

5.13 The object of the following procedures is to determine short term drift of the TCRO as well as to adjust the frequency. The adjustments are the COARSE and FINE controls on the rear panel. *Use only a non-metallic blade type adjustment tool for these adjustments.*

a. Set the counter controls as described in paragraph 5.8a.

b. Allow the counter to temperature stabilize for 72 hours before calibration. (It is not necessary to turn the power on during the warmup and stabilization period. The TCRO is an oven oscillator which operates from a separate +28 volt supply.) Set DISPLAY TIME to about 9 o'clock one hour before adjustment.

c. Connect a 1 or 5 MHz Frequency Standard to channel 1 of a dual channel oscilloscope. Trigger the oscilloscope on channel 1 only. Set the oscilloscope sweep rate to .02 μs per cm.

d. Connect a BNC cable to the counter INT OUT connector J106 on the rear panel. Set the REF switch S102 to the INT OUT position. Connect the other end of the BNC cable to the second channel of the oscilloscope. The oscilloscope display should indicate a stationary and a moving waveform. The moving waveform is the counter reference oscillator.

e. Remove the nylon cap screws. Adjust the COARSE adjustment (rear panel, see figure 6.8) and then the FINE adjustment until as near a completely stable waveform as possible is obtained. The channel 2 waveform will be drifting to the left or right. If the channel 2 waveform is moving to the left, the internal reference oscillator is higher in frequency than the frequency standard. If the channel 2 waveform moves to the right, the internal reference oscillator is lower in frequency than the frequency standard.

f. To determine the drift rate, measure the time it takes the oscilloscope pattern to drift the width of one cycle on channel 2. Note: 1 cycle equals 5 divisions on the oscilloscope. The oscillator drift can be determined from figure 5.1.

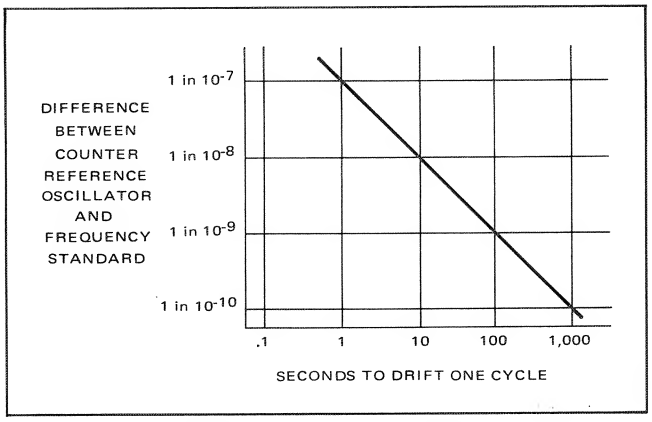


Figure 5.1 - Oscillator Drift

5.14 SIGNAL CONDITIONING CALIBRATION – CHANNEL A.

a. Set the controls as follows:

Control	Setting
A Slope	(+) Plus
A Coupling	AC
MULTIPLIER/TIMEBASE	1 second
A Trigger Level	PRESET
A Voltage Input Range	1
SEP/COM	SEP
FUNCTION	FREQ A
DISPLAY TIME	about 9 o'clock

b. Apply power to the counter 1 hour before adjustment. Do not remove the top or bottom covers during warmup.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Use a DC coupled oscilloscope with .5V/cm sensitivity to compare logic levels at MD1-12 and MD2-8 on the switch board assembly. Refer to figure 6.3, Switch Board Layout, for locations.

d. Adjust the ECL level pot R17A (figures 5.3 and 6.1) so the logic levels at MD1-12 are the same as the logic levels at MD2-8.

e. Connect a 150 MHz, 40 mV RMS signal to channel A input.

f. While observing the signal at MD1-12, switch the channel A slope between (+) plus and minus (–). Note the DC voltage shift between + and – slopes. Adjust the offset pot R20A for a minimum DC shift. Notice that with no DC shift, a permissible change in peak-to-peak amplitude may occur. The signal at MD1-12 is shown in figure 5.2. The signal output in either slope must be a minimum of .4 volts peak-to-peak.

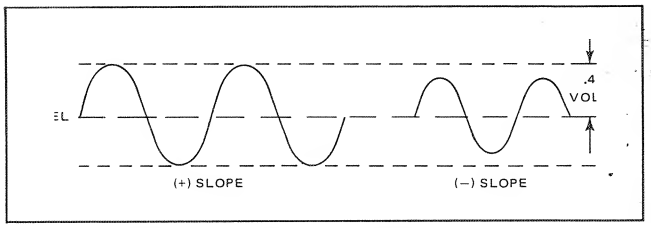


Figure 5.2 - Signal Conditioner Output

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are as follows:

50 mV RMS to 100 MHz, 100 mV RMS to 150 MHz.

g. Place channel A in – slope. Increase signal level to insure that the proper reading is displayed by counter. Incrementally decrease input signal level until an improper reading is observed. Then adjust R17A for the correct reading. Continue this process until maximum sensitivity is obtained.

i. Final check and adjustment should be completed after the unit is at ambient temperature with the top and bottom covers on.

5.15 SIGNAL CONDITIONING CALIBRATION – CHANNEL B

a. Set the Controls as follows:

Control	Setting
Slope A	+
Slope B	–
Coupling A	AC
Coupling B	AC
Trigger Level A	PRESET
Trigger Level B	PRESET
Input Range A	1
Input Range B	1
SEP/COM	SEP
FUNCTION	TIA
DISPLAY TIME	about 9 o'clock
MULTIPLIER/TIMEBASE	1 second

b. Apply power to the counter 1 hour before adjustment. Do not remove top and bottom covers during warmup period.

c. Apply a 10 MHz 100 mV rms signal to channel A input. Apply the same signal to a 10 dB Attenuator. Connect the output of the attenuator to channel B input.

d. Monitor the signal output of signal conditioner at ME0-6 on the Switch Board assembly. (figure 6.3)

e. Use a DC coupled oscilloscope with .5V/cm sensitivity and compare logic levels at ME0-6 and MC1-8 on the Switch board.

f. Adjust the ECL level control R17 (figures 5.3 and 6.1) such that the logic levels at ME0-6 are the same as the logic levels at MC1-8.

g. Incrementally decrease input signal level until an improper reading is observed. Then adjust R20 for the correct reading. Continue this process until maximum sensitivity is obtained.

h. Check the sensitivity over the band in both + and – slopes. Nominal sensitivities are: 0 – 10 MHz, 50 mV RMS.

i. Final check and adjustments should be completed after the counter is at ambient temperature with both top and bottom covers on.

5.16 PERIODIC MAINTENANCE.

5.17 To determine if the counter is operating properly within specifications, perform the performance check (Section 3).

5.18 ACCESS TO PC BOARDS.

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC Power source.

5.19 To remove top and bottom covers, proceed as follows:

a. Remove power cord.

> **WARNING**
>
> The power supplies are still active as long as the power cord is plugged into the power AC source.

b. Loosen the four captive screws, one at each corner of the top cover and remove the top cover.

c. Turn the counter upside down. Loosen the four captive screws on the bottom cover and remove the bottom cover.

5.20 PCB REMOVAL.

5.21 When removing the printed circuit board for replacement, repair, and servicing, always remove the AC power cord before disassembly. Refer to figure 5.23, page 5-15 for assembly location.

5.22 RF Assembly (figure 6.12 or 6.14).

a. Remove the six #4 phillips-head screws around the outer edge of the assembly.

b. Disconnect the two subminiature RF connectors.

c. Disconnect P10 at the rear of the counter.

d. On instruments having option 030, remove the five #4 screws holding the RF shield on the component side. Remove shield.

> **CAUTION**
>
> The R.F. assembly is very sensitive to component movement. Do not move any components or recalibration will be necessary.

5.23 Signal Conditioning Assembly (figure 6.1).

a. Remove the trigger level knobs and the input range knobs.

b. Remove the two #6 phillips-head screws on the top of the signal conditioner and one #6 phillips-head screw on the bottom.

c. Remove the subminiature R.F. connectors.

d. Remove the two #6 phillips-head screws holding cable clamps on the cable between the signal conditioner and P9. Remove P9 and remove the assembly.

e. To service the attenuator switch, remove the four #4 phillips-head screws located at each corner of the printed circuit board. The printed circuit board can be moved away from the switch assembly for servicing.

5.24 Readout Assembly (figure 6.5).

a. Remove the interconnection printed circuit assembly from J4.

b. Remove P1 at the left rear of the assembly.

c. Remove P5 and the FUNCTION knob at the right front side.

d. Remove the seven #6 phillips-head screws (one in the center and six around the perimeter of the board). The Readout assembly can now be removed.

5.25 Switch Board Assembly (figure 6.3).

a. Remove the interconnection printed circuit assembly from J2.

b. Unscrew the subminiature RF connectors from the Signal Conditioning assembly and the RF assembly.

c. Remove P3 from J3.

d. Remove the six #6 phillips-head screws, two in the center and four around the perimeter of the printed circuit board. Remove the switch board assembly.

5.26 COMPONENT REPLACEMENT.

5.27 When replacing a circuit board component, use a low heat soldering iron (25 watt). Heat must be used sparingly as damage to the circuit foil may result. Plated-thru holes may be cleaned with a solder remover while heat is applied. The connection should be cleaned with a cleaning solution after the component removal and replacement.

5.28 Integrated Circuit Replacement.

5.29 Integrated circuits can be unplugged and substituted without soldering or assembly removal. The use of special tools to remove IC is not recommended. To remove an IC, place both thumbs on top of the IC and both index fingers at the ends of the IC. Gently rock the IC upward in small steps. Do not "pop" it out in one motion. To replace an IC, be sure the notched end points the same direction as the other ICs on the board. Straighten any bent pins. Align the pins on the IC with the holes in the socket and press the IC in firmly using one or two fingers.

5.30 Identification of Parts.

5.31 All parts are listed in the parts list, Section 7, by assembly. Reference designators are called out on the schematic and can be found on the layout drawings. The Dana part number and description are given in the parts list. All integrated circuits used in the counters are standard 7400 series TTL and ECL that can be purchased from your local supplier. Special parts may be obtained from Dana by writing or calling Product Service at 714-833-1234 collect in California.

5.32 Parts Location.

5.33 The integrated circuits on the Readout and Switch board assemblies are layed out on a grid pattern. Looking at the readout or switch board from the front, the ICs are numbered across the board from left to right, 1 through 12; top to bottom, A through F. Other components are designated by circuit and can be located by the schematic and layout drawing.

5.34 TROUBLESHOOTING.

5.35 This section describes methods for identifying counter troubles and determining the specific corrective action that should be taken. Familiarity with the Operation (Section 3) and Theory of Operation (Section 4) makes troubleshooting easier.

5.36 A malfunction can be rapidly defined to one of four categories.

a. Apparent trouble which is really a misplaced control setting or an erratic external signal.

b. Visual damage such as printed circuit board broken, etc.

c. Analog trouble which requires troubleshooting and component replacement.

d. Digital trouble which requires troubleshooting and IC replacement.

5.37 Repairs which require replacement of soldered-in components can be accomplished rapidly, but caution should be taken against soldering with improper procedures. Solder damage to the printed circuit boards is not covered by Dana's warranty.

5.38 Apparent Troubles.

5.39 Apparent troubles are those which appear to be equipment malfunctions, but are really controls which are misadjusted.

5.40 The counter will not operate if a function is incorrectly selected. For instance, if the unknown frequency is connected to input C and FREQ A function is selected, there will be no reading. Be sure the FUNCTION switch is in the proper mode. If the function has been changed, depress RESET to start a new reading in the new function.

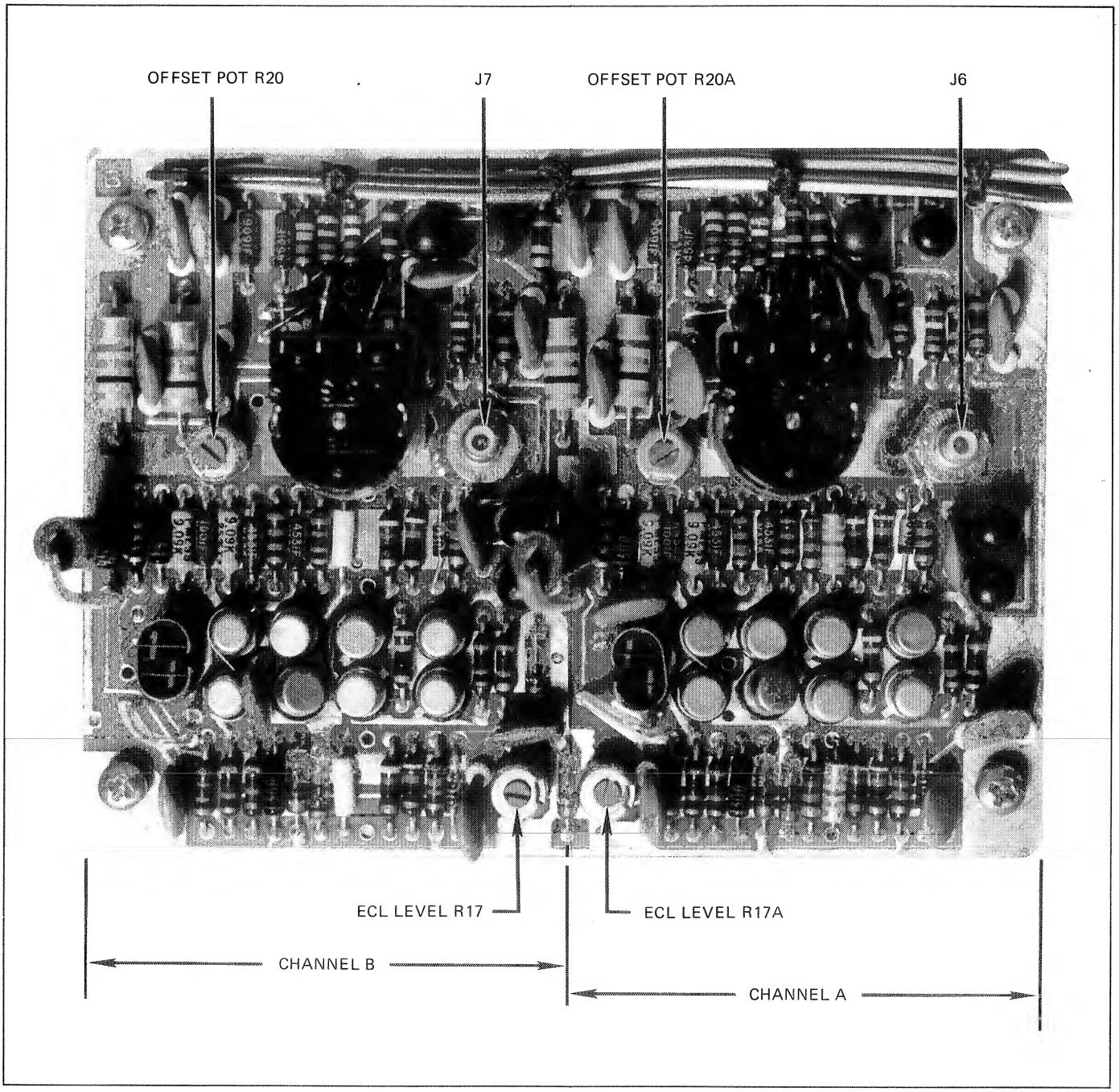


Figure 5.3 - Signal Conditioning Adjustments

Table 5.3 - Front Panel Symptoms

Type of Problem	Refer to Paragraph:
Readout	5.49
Remote Operation	5.64
Self-Check Mode	5.68
Frequency A Mode	5.70
Period Mode	5.73
Period Average Mode	5.75
Frequency C (Not in 8010B)	5.77
Totalize Mode	5.80
Time Interval Mode	5.82
A/B (Ratio) Mode	5.85
Time Interval Average Mode	5.88

5.41 If the input voltage range or trigger level are improperly set, inputs A or B will not operate. Be sure that a measurable signal is present and that controls are set properly for that signal.

5.42 When input C is used (not in 8010B), the automatic gain control will inhibit readings of signals which are less than 50 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band (1.0 MHz to 550 MHz). With Option 030, the automatic gain control will inhibit readings of signals which are less than 1 mV and greater than 1V RMS. Signals will be inhibited if they are outside the measurable band for Option 030 (10 MHz to 500 MHz).

5.43 Due to the sensitivity of input C, open leads which might act as an antenna can cause improper readings. If open leads or probes must be used, it may be necessary to insert a low-pass filter at the counter input to discriminate against unwanted signals received through radiation. Unshielded input signals can cause unwanted signals to override the desired signal. The proper operation of input C can be verified by connecting a signal generator directly to the counter through a shielded 50-ohm terminated cable. Once proper counter operation has been verified, unwanted external signals can be attenuated with a low-phase filter.

5.44 Visual Check.

5.45 A possible source of malfunction could be short or open circuits which disable portions of the counter or load down the power supply, or both. Often these short-circuits can be located by visual inspection. A quick visual check of the counter with the covers removed may reveal foreign metal parts, frayed cable braid, discolored components, etc. which can be easily corrected. Visual checks can be more meaningful after the trouble has been localized.

5.46 Open circuits can also be located visually. Examine connector and wire harnesses for obvious breakage or opens.

5.47 Front Panel Symptoms.

5.48 Localize the trouble to one of the categories listed in table 5.3; then proceed to the appropriate paragraph and follow the suggested procedure.

5.49 READOUT INOPERATIVE.

5.50 If the readout tubes and annunciators do not light, a failure in the 150V supply is indicated. Check the line fuse. It should be .75 amp, 3 AG. If in doubt, measure the AC source at the power transformer T101 to assure that power is getting to the counter. Check the 150-volt supply as follows.

a. Turn power off; remove the power cord at the rear of the counter. The supplies are still active even with the power switch turned off. Remove the top cover and reconnect the power cord.

b. Connect a voltmeter to either side of resistor R60, 3.9K, 3W (figure 6.5). Connect the other lead of the voltmeter to ground (negative side of capacitor C7). The voltage should read about 150 volts DC.

c. Note the action that occurs when the DISPLAY TIME switch is moved clockwise from the PWR OFF position. If the voltage goes very low or to zero, there is a short in the 150V line. If no voltage is present at either side of R60, check the following: R61 (located under C6), C5, CR5 through CR8, and T101.

d. Remove P1 and check for 180 volts RMS AC at points P1-E (blue transformer lead) and P1-D (violet transformer lead).

e. If the high voltage is still not present, check the wire harness for opens or shorts. If no opens or shorts are found, T101 may be defective.

f. If the high voltage is present, reconnect P1 and recheck the 150 volt lines. If the 150 line loads down, locate and eliminate the short on the readout board.

5.51 READOUT TUBE BLURRING.

5.52 If all readout tubes blur, a faulty +5-volt supply voltage is indicated. The 5-volt supply is affected by the other power supplies, so they must all be checked.

5.53 Series regulator transistors for the +5-volt and ±18-volt supplies are mounted on a heatsink on the rear panel. A short to ground in the −18-volt supply turns off the +5-volt and +18-volt supplies. Instruments equipped with Option 200 have a separate +28-volt supply and regulator. A short in this supply also affects the other voltages. It can be measured at J4-X.

5.54 Check the power supply voltages at the points listed below. Refer to figure 6.6 for voltage levels within the power supply.

Power Supply	Measurement Point (figure 6.5)
+5V	J4-20 or CR40 anode
+18V	Cathode of CR40
−18V	Anode of CR22

5.55 If any of the power supply voltages are abnormal, disconnect the load to isolate the trouble to the supply or to the load. If the voltage returns to normal, reconnect the load and selectively unplug the interconnection board, the signal conditioning board, and the prescaler until the source of the overload is located.

5.56 If the trouble appears in only one readout tube, a bad integrated circuit (IC) driver or a bad readout tube is indicated. Driver IC's are 7441's in Row F directly behind the readout tubes. Remove power, and exchange the 7441 behind the bad readout with the neighboring driver. If the trouble moves with the driver (7441), replace the 7441 driver. If the trouble stays when the driver is moved, replace the readout tube. If none of the above solves the problem, inspect the circuit near the tube, driver, or quad latch (7475) for shorts or opens.

5.57 ANNUNCIATORS INOPERATIVE.

5.58 The "gate" and units annunciators are located in front of and below the readout tubes (figure 6.5). They are operated from the +150-volt and +5-volt power supplies. If none of the annunciators light, the power supply is probably faulty. Perform the power supply checkout procedures described in paragraph 5.49.

5.59 If the GATE annunciator does not operate, proceed as follows:

a. Set DISPLAY TIME counterclockwise, just short of the PWR OFF position.

b. Set FUNCTION switch to the CHECK mode.

c. Depress the 100 ms TIMEBASE switch (the GATE light should flash at approximately 130 ms intervals).

d. With an oscilloscope, check at the cathode of CR1 for a pulse going from zero to +4.0 volts. If the pulse is not present, check at J2-4 (see circuit, figure 5.4).

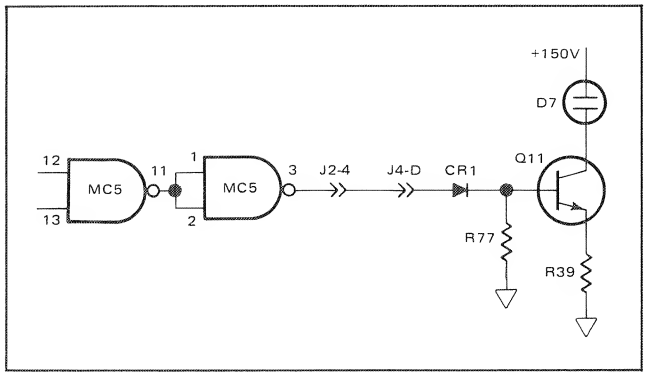


Figure 5.4 - Gate Annunciator

e. If the pulse is not present at J2-4, check the control logic on the Switch board assembly. Verify first that a "start" pulse is being generated.

5.60 If one of the units annunciators does not light, refer to table 5.4. In the table, voltage levels at the inputs and output of gates are listed. If a level differs by ±10% from that listed, the trouble is located between the correct level and the incorrect level. Integrated-circuit drivers in each circuit may be unplugged and exchanged with one of the same type known to be good. If a driver becomes shorted, the corresponding annunciator remains "on". If the driver is open, the annunciator remains "off".

5.61 DECIMAL POINT MALFUNCTION.

5.62 Should any one decimal point not turn on, perform the following decimal point check:

a. Set the FUNCTION switch to FREQ C. Select the 1 μs timebase. No decimal point should be lit. If one is lit, try substituting the readout with the one

Table 5.4 - Units Annunciators Troubleshooting

Annunciator	Function	Select Timebase/Multiplier	Measurement Point	Normal Level	Figure No.
μsec	PERIOD Mode	1 μs	E54 MB11-8	≥2.0 volts	5.5
			MB11-10 MC12-8	≤0.8 volts	
			MB11-11 MB12-3	≥2.0 volts	
			MB12-1	≤0.8 volts	
			MB12-2	≤0.8 volts	
msec	PERIOD Mode	10 μs	E50 MD10-12	≤2.0 volts	5.6
			MD10-13 MD12-8	≤0.8 volts	
			MD12-2	≥2.0 volts	
			MD12-3	≥2.0 volts	
nsec	PER AVG Mode	10^6	E52 MD11-11	≥2.0 volts	5.7
			MD11-13 MC11-8	≤0.8 volts	
			MD11-12	≥2.0 volts	
			MD11-8	≥2.0 volts	
sec	PERIOD Mode	10 ms	E51 MD11-3	≥2.0 volts	5.8
			MD11-1 MC11-6	≤0.8 volts	
			MC11-2	≥2.0 volts	
			MC11-3	≥2.0 volts	
KHz	FREQ A Mode	10s	E53 MB12-8	≥2.0 volts	5.9
			MB12-9 MB12-6	≤0.8 volts	
			MB12-4	≥2.0 volts	
			MB12-5	≥2.0 volts	
MHz	FREQ A Mode	1s	E49 MD10-2	≥2.0 volts	5.10
			MD10-1 MC9-8	≤0.8 volts	
			MC9-1 MA12-6	≥2.0 volts	
			MA12-5 MB8-3	≥2.0 volts	
			MB8-1	≥2.0 volts	
			MB8-2	≥2.0 volts	
			MC9-13	≥2.0 volts	

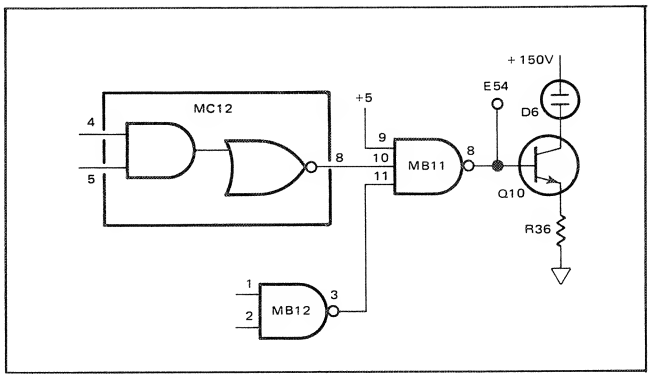


Figure 5.5 - "µsec" Annunciator

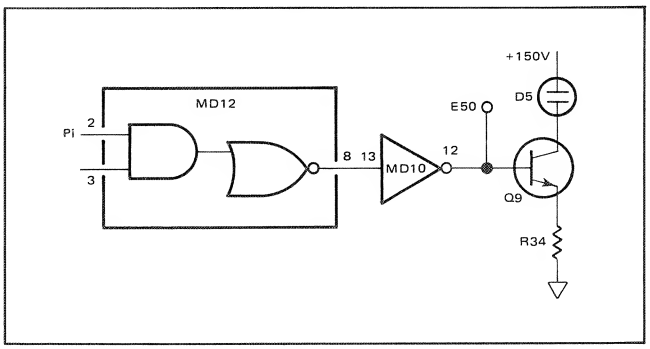


Figure 5.6 - "msec" Annunciator

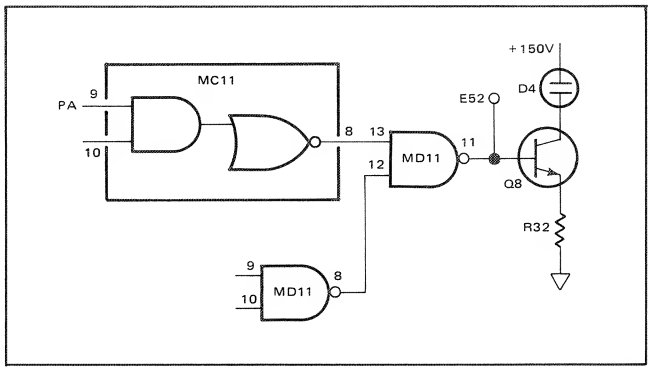


Figure 5.7 - "nsec" Annunciator

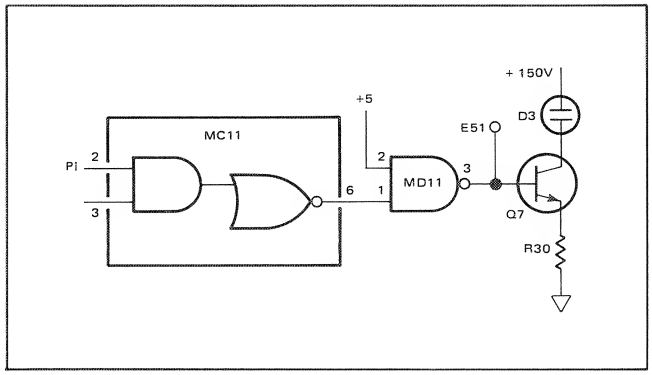


Figure 5.8 - "sec" Annunciator

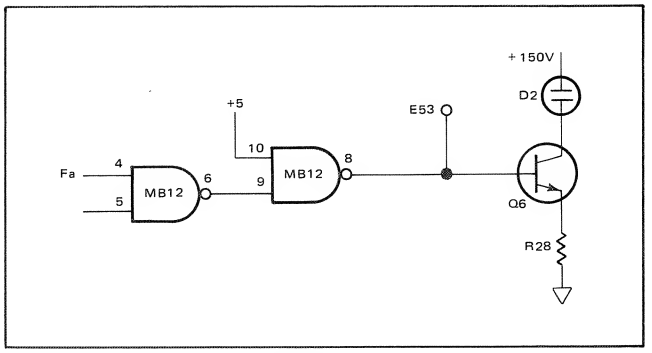


Figure 5.9 - "KHz" Annunciator

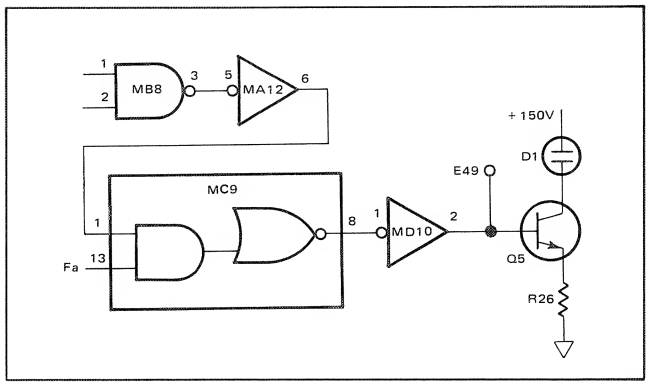


Figure 5.10 - "MHz" Annunciator

next to it. Each decimal point is driven by a transistor which, if open or shorted, causes a decimal point to remain off or on continuously.

b. Depress the 10 µs to 100s TIMEBASE switches; the decimal point should light as shown in table 5.5.

5.63 Procedures for signal tracing through the DP logic are listed in table 5.6.

Table 5.5 - Decimal Point Placement

Timebase	Decimal Point Display								
	V9	V8	V7	V6	V5	V4	V3	V2	V1
10 µs	0	0	0	0	0	0	0	0	.0
100 µs	0	0	0	0	0	0	0	.0	0
1 ms	0	0	0	0	0	0	.0	0	0
10 ms	0	0	0	0	0	.0	0	0	0
100 ms	0	0	0	0	.0	0	0	0	0
1s	0	0	0	.0	0	0	0	0	0
10s	0	0	.0	0	0	0	0	0	0
100s	0	.0	0	0	0	0	0	0	0
	↑	DP8	DP7	DP6	DP5	DP4	DP3	DP2	DP1

Models with Option 004 (9th digit)

Table 5.6 - Troubleshooting Procedure - DP Logic

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP1	10 μs	E70 MC7-6	≥2.0 volts	5.11
		MC7-5 MA9-8	≤0.8 volts	
		MA9-4 MA9-5	≥2.0 volts	
DP2	100 μs	E71 CR26 anode CR27 anode	≥2.0 volts	5.12
		MC7-11	≥2.0 volts	
		MC7-12 MC8-6	≥2.0 volts	
		MC7-13 MB9-8	≤0.8 volts	
		MB9-4 MB9-5	≥2.0 volts	
DP3	1 ms	E72 MB7-12	≥2.0 volts	5.13
		MB7-13 MC9-6	≤0.8 volts	
		MC9-4 MC9-5	≥2.0 volts	
DP4	10 ms	E73 MB7-6	≥2.0 volts	5.14
		MB7-5 MA10-8	≤0.8 volts	
		MA10-4 MA10-5	≥2.0 volts	
DP5	100 ms	E74 MB7-4	≥2.0 volts	5.15
		MB7-3 MB10-8	≤0.8 volts	
		MB10-2 MB10-3	≥2.0 volts	
DP6	1s	E75 MC7-8	≥2.0 volts	5.16
		MC7-9 MC10-6	≤0.8 volts	
		MC10-2 MC10-3	≥2.0 volts	
		MC8-8 MC7-10	≥2.0 volts	

Table 5.6 - Troubleshooting Procedure - DP Logic (continued)

Decimal Pt.	Select Timebase	Measurement Point(s)	Normal Level	Figure No.
DP7	10s	E76 MB7-2	≥2.0 volts	5.17
		MB7-1 MC10-8	≤0.8 volts	
		MC10-1 MC10-13	≥2.0 volts	
		MA12-12	≥2.0 volts	
DP8	100s	E77 MB7-10	≥2.0 volts	5.18
		MB7-11 MC8-3	≤0.8 volts	
		MC8-1 MC8-2	≥2.0 volts	
		MA7-10	≥2.0 volts	

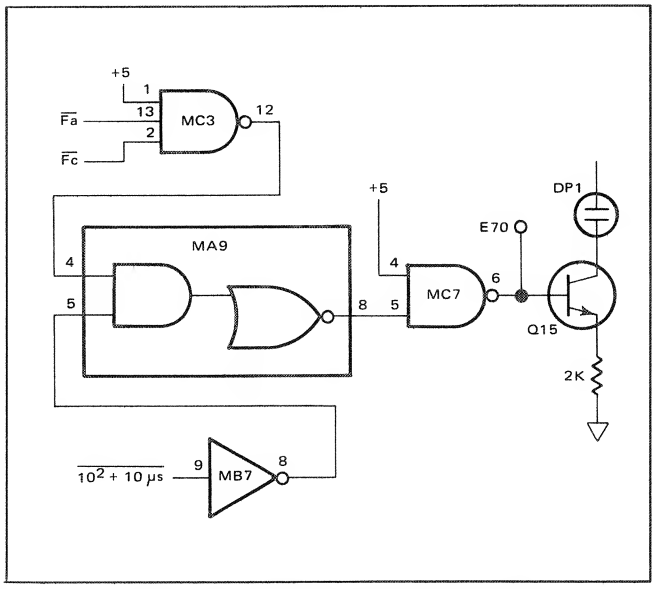


Figure 5.11 - DP1 Decimal Point Logic

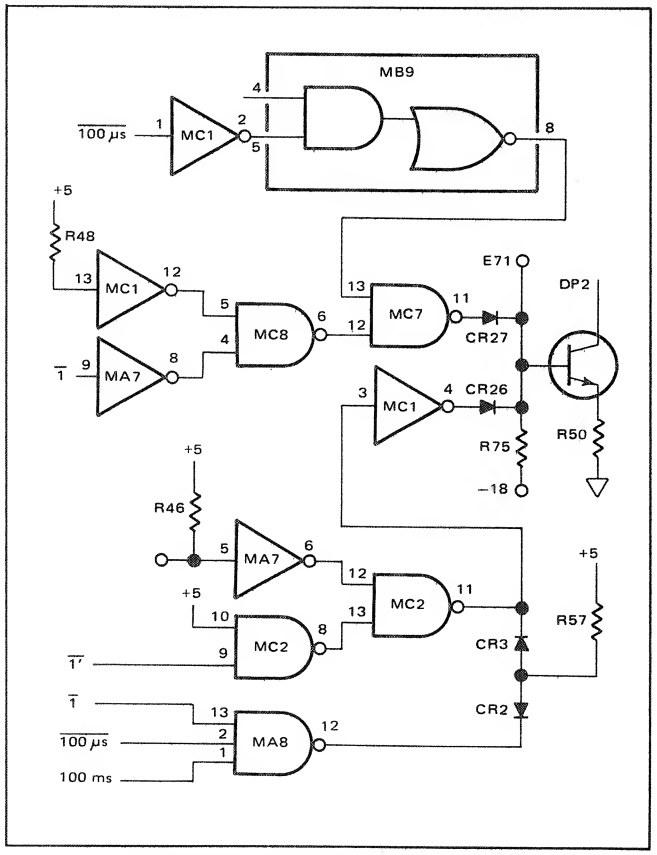


Figure 5.12 - DP2 Decimal Point Logic

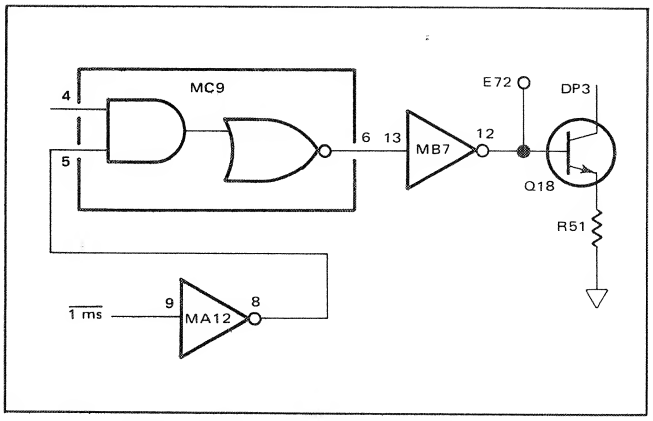


Figure 5.13 - DP3 Decimal Point Logic

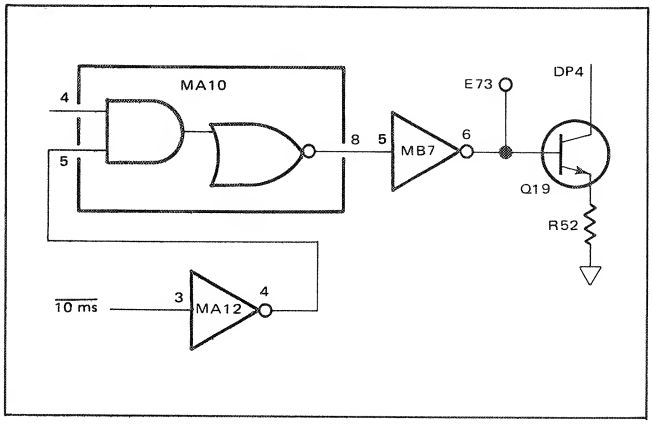


Figure 5.14 - DP4 Decimal Point Logic

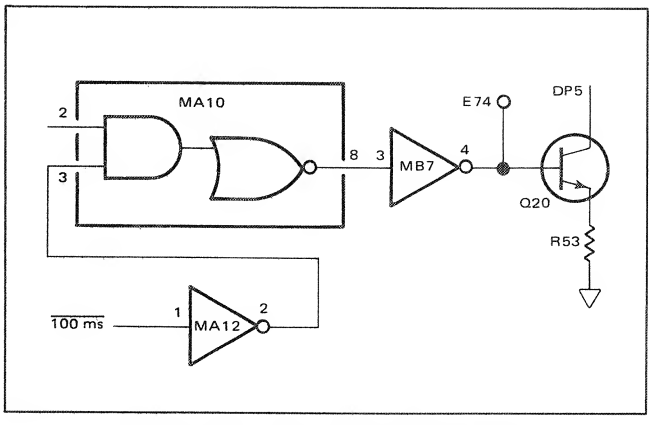


Figure 5.15 - DP5 Decimal Point Logic

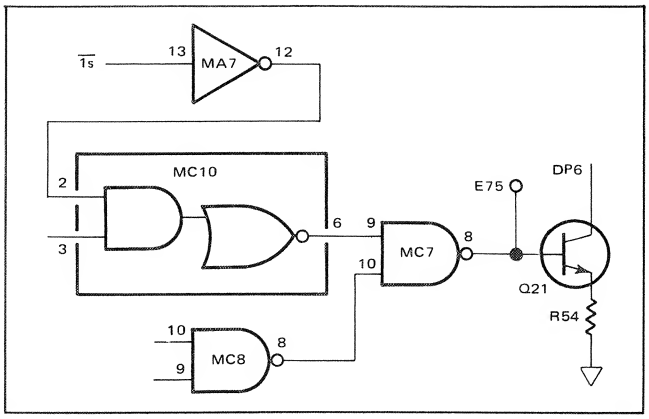


Figure 5.16 - DP6 Decimal Point Logic

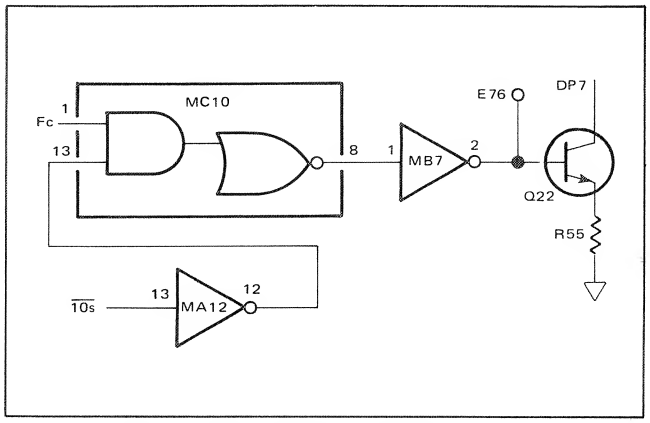


Figure 5.17 - DP7 Decimal Point Logic

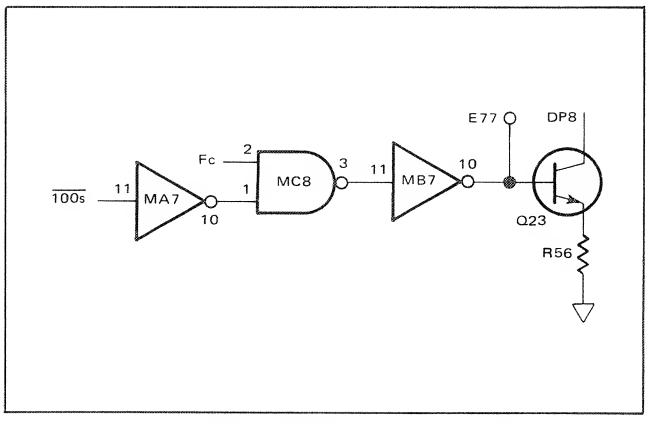


Figure 5.18 - DP8 Decimal Point Logic

5.64 Faulty Remote Operation.

5.65 Normally, problems occurring with the remote programming option occur also in local operation. Verify that transistor Q7 on the Switch board turns off with REMOTE selected. If Q7 operates properly, a malfunction can be traced by following the procedures for troubleshooting a specific operating mode. Also verify that there are no opens or wiring errors in the external circuits.

5.66 Faulty Operation In One Mode.

5.67 Figures 5.25 through 5.33 show the signal flow through the instrument in each mode of operation. Logic levels are given at significant check points to assist in signal tracing.

5.68 CHECK MODE (Figure 5.25).

5.69 In Check mode, the reference oscillator frequency is routed to the counting decades and to the timebase decades.

5.70 FREQUENCY A MODE (Figure 5.28).

5.71 The signal for Frequency A mode is routed through the Signal Conditioning assembly where the trigger slope and trigger point are selected. Attenuation of the signal also takes place in the attenuator section of the signal conditioning. Frequency A (f_a) is routed to the counting decades. The time that the counting decades are allowed to count is controlled by the Reference Oscillator, Timebase Decades, and the Control Logic. Be sure that the FUNCTION switch is positioned to FREQ A and that the range and trigger level controls are set correctly.

5.72 Connect an oscilloscope to E2 and E1 on the Switch board assembly. Connect a signal to the Frequency A input and adjust the counter accordingly. An ECL square wave should be seen varying between 3.4V and 4.2 volts dc. Try moving the trigger level control over its range. If no signal is found, the trouble is in the Attenuator or Signal Conditioning Module. Refer to the schematic of the Signal Conditioning module for troubleshooting (figure 6.2).

5.73 PERIOD MODE (Figure 5.26).

5.74 The signal in the Period mode is routed through the Attenuator and the Signal Conditioning assembly where the trigger slope and trigger level are selected. The signal (f_a) is routed to the Control Logic which controls the time that the counting decades are allowed to count the Reference Oscillator or a frequency division of the Reference Oscillator. Follow the procedure in paragraph 5.72. If the signal is present at E2 and E1, refer to the Period Signal Flow schematic for gate levels and signal flow.

5.75 PERIOD AVERAGE MODE (Figure 5.27).

5.76 The signal in Period Average mode is routed through the Attenuator to the Signal Conditioning assembly and to the Multiplier Timebase Decades. The output of the Timebase Decades (f/n) goes to the start/stop logic and on to the Control Logic which controls the counting decades. The Reference Oscillator is routed to the fast counting decades. The counting decades are controlled by Δt. Δt's time is determined by f_a and the multiplier selected on the front panel. Follow the procedure in paragraph 5.72. If the signal is present at E_2 and E_1, refer to the Period Average Signal Flow schematic for gate levels and signal flow.

5.77 FREQUENCY C MODE (Figure 5.29, not in 8010B).

5.78 Frequency C is much like Frequency A operation. The signal is connected to the Frequency C input and routed into the Frequency C RF Assembly. The signal is amplified. The amplification is controlled by an automatic gain control circuit (AGC). The signal is divided by two through a discrete flip-flop and divided again by two through a ECL flip-flop. The signal is routed to E4 and E3 on the Switch board assembly. The signal (f_c) goes to a ECL gate and to the counting decades. The Reference Oscillator is gated through to a divide-by-four flip-flop to the Timebase Decades.

5.79 To determine if the Frequency C signal reaches the Switch board, connect an oscilloscope to E4 and E3 on the Switch board. Set the FUNCTION switch to FREQ C. Connect a signal to Input C. A ECL square wave should be seen on the oscilloscope varying between 3.4V and 4.2 volts dc. If no signal is found, the trouble is in the Frequency C RF assembly. Refer to figure 6.12 or 6.13 or figures 6.14 and 6.15 for Option 030 (1 mV, 10 MHz – 500 MHz) for the schematic of the RF assembly.

5.80 TOTALIZE MODE (Figure 5.30).

5.81 The signal in the Totalize mode is routed through the A input to the Attenuator and Signal Conditioning Module where the trigger level and slope are selected. The output of the Signal Conditioner is gated to the counting decades. The counting decades are controlled by the manual start/stop circuit which develops Δt, the gate time for the

count. The input signal divided by 10 ($f_a/10$) is routed to the Timebase Decades and to the scaled output connector for external use.

5.82 TIME INTERVAL MODE (Figure 5.31).

5.83 The signals in the Time Interval mode are routed through the A and B inputs to the A and B Signal Conditioning Modules. The Signal Conditioning circuits determine the trigger points and trigger slope. The output of A is at E2 and E1 on the Switch board. The output of B is at E6 and E5 on the Switch board. The Reference Oscillator is gated to the Multiplier Timebase Decades. The Multiplier Timebase Decades are gated to the counting decades. The counting decades are controlled by the Control Logic which is controlled by the stop/start logic. The signal from input A determines the start time and the input B signal determines the stop time. The start and stop circuits define the gate time.

5.84 Verify that the input controls are set correctly. Observe E2 and E1, and E6 and E5 to determine that a square wave pulse is being generated at the correct time. If a signal is not present, refer to the Signal Conditioning schematic, figure 6.2.

5.85 A/B (RATIO) MODE (Figure 5.32).

5.86 The signals in the Ratio mode are routed through the Inputs A and B. The signal from Input A goes to the Attenuator and Signal Conditioning circuits where the trigger level and slope are selected. The output of the A Signal Conditioner (f_a) is routed to the counting decades. The output of B Signal Conditioner (f_b) is routed to the Multiplier Timebase Decades and to the Control Logic. The Control Logic starts and stops the counting decades.

5.87 Verify that there is a signal at the output of the A Signal Conditioner (E2, E1). Verify that there is also a signal at the output of the B Signal Conditioner (E6, E5). If either of these signals are missing, refer to the Signal Conditioner schematic, figure 6.2.

5.88 TIME INTERVAL AVERAGE MODE (Figure 5.33).

5.89 The signals in the Time Interval Average mode are routed through Inputs A and B. The signals are attenuated at the Attenuator. The trigger level and the slope are selected in the A and B signal conditioners. Signals f_a and f_b are routed to the Switch board at points E2 and E1 (A) and E6 and E5 (B). Signal f_a is routed to two type-D flip-flops. The signal is synchronized with the Reference Oscillator. When signal f_a goes high, the reference clock enables the counting decades. Signal f_b is synchronized with the Reference Oscillator and disables the reference clock to the counting decades at the end of the incoming signal. Signal f_b also produces f_b SYN which goes to the Timebase Decades. Signal f_b SYN is generated once per measurement period. Thus, the Timebase Decades count f_b SYN. Depending on the multiplier selected, 1 to 10^9, one measurement or 1000 million measurements will be made and averaged.

5.90 Verify that the signals f_a and f_b, at ECL levels, appear at points E2 and E1 (A), and E6 and E5 (B). If a signal is not present, check the controls for proper setting. Refer to figure 6.2 for schematic of the Signal Conditioner. If both signals f_a and f_b are present, refer to the signal flow schematic.

5.91 Troubleshooting The Signal Conditioning Assembly.

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC Power source.

5.92 For disassembly refer to paragraph 5.23. Follow the calibration procedures in paragraphs 5.14 and 5.15 (dual channel). If this does not reveal the problem, refer to the schematic, figure 6.2. Voltage levels and signal level are given on the schematic.

5.93 Channel A and channel B (except on 8020B) are schematically the same. The reference designators are suffixed with an "A" in the channel A circuits. To verify that Q1 and Q10 are matched to each other, proceed as follows:

a. Ground the bases of Q4 and Q8.

b. Measure between the bases of Q2 and Q9. Verify the operation of R20; the voltage should vary from negative, through zero, to positive. If this voltage range cannot be obtained, either Q1 and Q10 are not matched or there is a component failure in the circuit.

5.94 The following pairs of transistors in this circuit are matched as indicated.

Q4 and Q8; V_{be} (base-to-emitter voltage)

Q2 and Q9; V_{be} (base-to-emitter voltage)

Q1 and Q10; R_{ds} (resistance, drain-to-source)

5.95 Troubleshooting The RF Assembly.

5.96 For disassembly, refer to paragraph 5.22. Note: *Do not move any components unless that component is known to be defective.* The RF Assembly is very sensitive to component location. Recalibration will be required if a component is replaced in a critical area. Voltage levels are

given on the schematic figures 6.13 or 6.15. However, it is recommended that the RF assembly be returned to Dana's Product Service for repair and calibration.

5.97 BASIC LOGIC DEFINITION.

5.98 TTL Logic.

5.99 A majority of the integrated circuits used in the 8000B counters are TTL type integrated circuits. TTL circuits operate up to ≅15 MHz. The basic Nor function is shown in figure 5.19. Logic levels are:

Logical 0: ≤.8V Logical 1: ≥2.0V

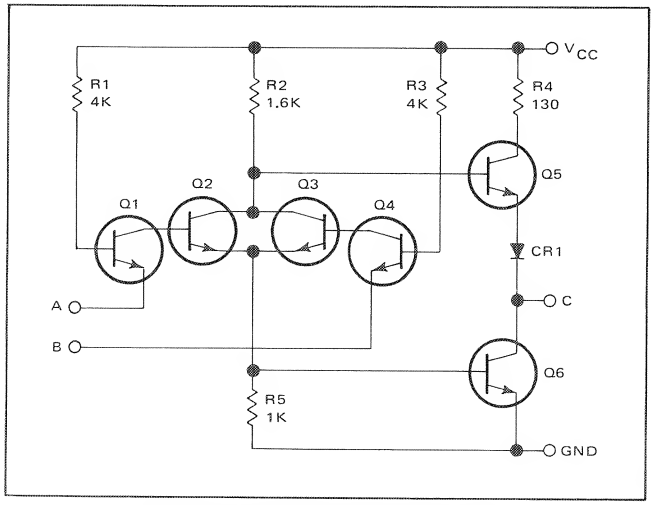


Figure 5.19 - Basic TTL Nor Gate

5.100 The Nor gate is comprised of six transistors. The two input transistors, Q1 and Q4, are used as diode or gates (figure 5.20). Transistors Q2 and Q3 are voltage phase inverters. Transistors Q5 and Q6 form a totem-pole output. The totem-pole circuit has a low output resistance for both a high and low level.

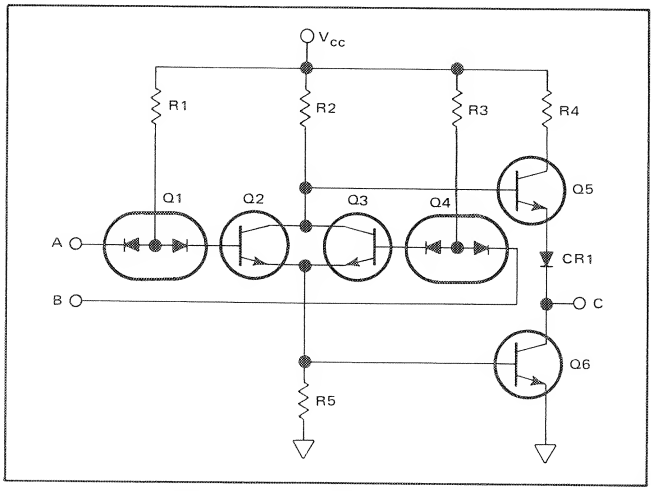


Figure 5.20 - Equivalent Circuit

5.101 Assume a Logical "0" level exists at both A and B inputs. Transistor Q1 and Q4 are conducting. Therefore, the collectors of Q1 and Q4 are at logical "0" level. The logical "0" level from the collectors of Q1 and Q4 are applied to the bases of Q2 and Q3 causing them to turn off. The collectors of Q2 and Q3 are connected together and to the base of Q5. The logical "1" on the base of Q5 causes Q5 to conduct. Output C is connected to the emitter of Q5 via CR1. Diode CR1 prevents an indeterminate output. The output of the Nor gate is two diode drops (1.4V) lower than the base voltages of Q5 or 3.6V.

5.102 Assume a logical "1" level is applied to input A. Base current for Q2 is supplied through R1 and the base-collector junction of Q1. Transistor Q2 is turned on. The collector of Q2 is connected to the base of Q5 and turns Q5 off. The emitter of Q2 is connected to the base of Q6. Q2 supplies base current to Q6 base; therefore Q6 is turned on and output C is low.

5.103 A logical "1" level applied to either or both inputs A or B result in a logical "0" level at output C. The truth table is shown in table 5.7.

Table 5.7 - Truth Table

A	B	C
1	1	0
1	0	0
0	1	0
0	0	1

5.104 Emitter Coupled Logic (ECL).

5.105 BASIC NOR FUNCTION.

5.106 A number of ECL integrated circuits are used in the counter. ECL circuits are used wherever high-speed switching is required. The basic Nor function is shown in figure 5.21. Logic levels used are:

Logical 0: 3.5V Logical 1: 4.2V

5.107 The gate is comprised of differential amplifier Q2 and Q3, input transistors Q1 and Q2, and emitter follower output transistor Q4. Transistor Q3 and resistors R3 and R4 form a fixed bias circuit.

5.108 Assume Logical "0" levels exist at both A and B inputs. Transistors Q1 and Q2 are cut off; therefore, the collectors of Q1 and Q2 are at a logical "1" level. The logical "1" level from the collectors of Q1 and Q2 is applied

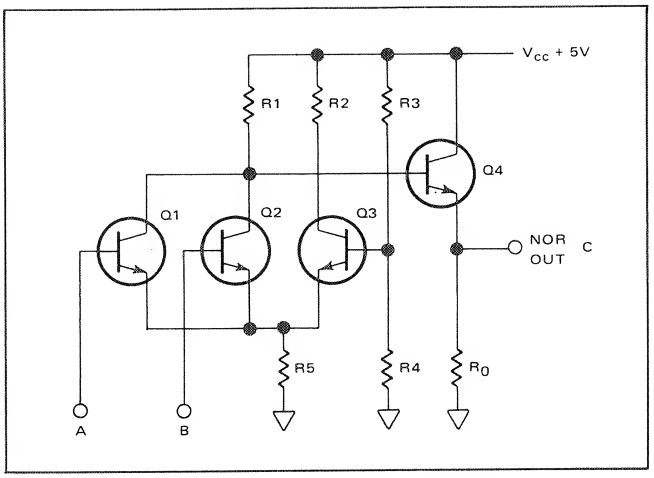


Figure 5.21 - Basic ECL Nor Gate

to the base of Q4, causing Q4 to conduct. The output at the emitter of Q4 is a logical "1" level (output C).

5.109 Assume that a logical "1" level is applied to input A. Transistor Q1 conducts and a logical "0" level results at the Q1 collector due to the drop across R1. The logical "0" level is applied to the base of Q4 causing Q4 to cut off providing a logical "0" level at output C.

5.110 A logical "1" level applied to either or both input A or B results in a logical "0" level at output C. The circuit therefore performs a Nor function; the truth table is shown in table 5.8.

Table 5.8 - ECL NOR Truth Table

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

5.111 DIODE GATE.

5.112 The purpose of a diode gate (figure 5.22) is to control a ECL level signal with a TTL gate. The diode gate is much faster than TTL logic and speed is required in these circuits. Diode CR2 is always in forward conduction with the current provided through resistor R2 from V. The state of CR1 depends on the output of TTL gate. If the TTL gate is high, the CR1 conducts. If the TTL gate is low, then CR1 is reverse-biased and the signal is not transferred from

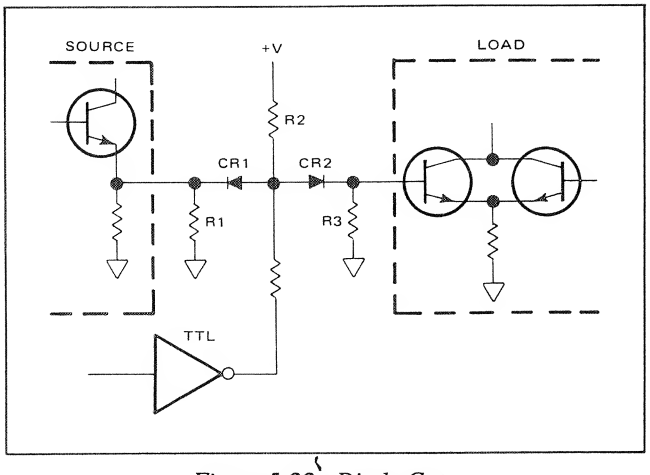


Figure 5.22 - Diode Gate

the source to the load. If the output of the TTL gate and CR1 is forward biased, a low insertion loss signal path is provided between the source and the load. DC levels are maintained between the source and load as shown in table 5.9 due to CR1 and CR2 being connected back-to-back.

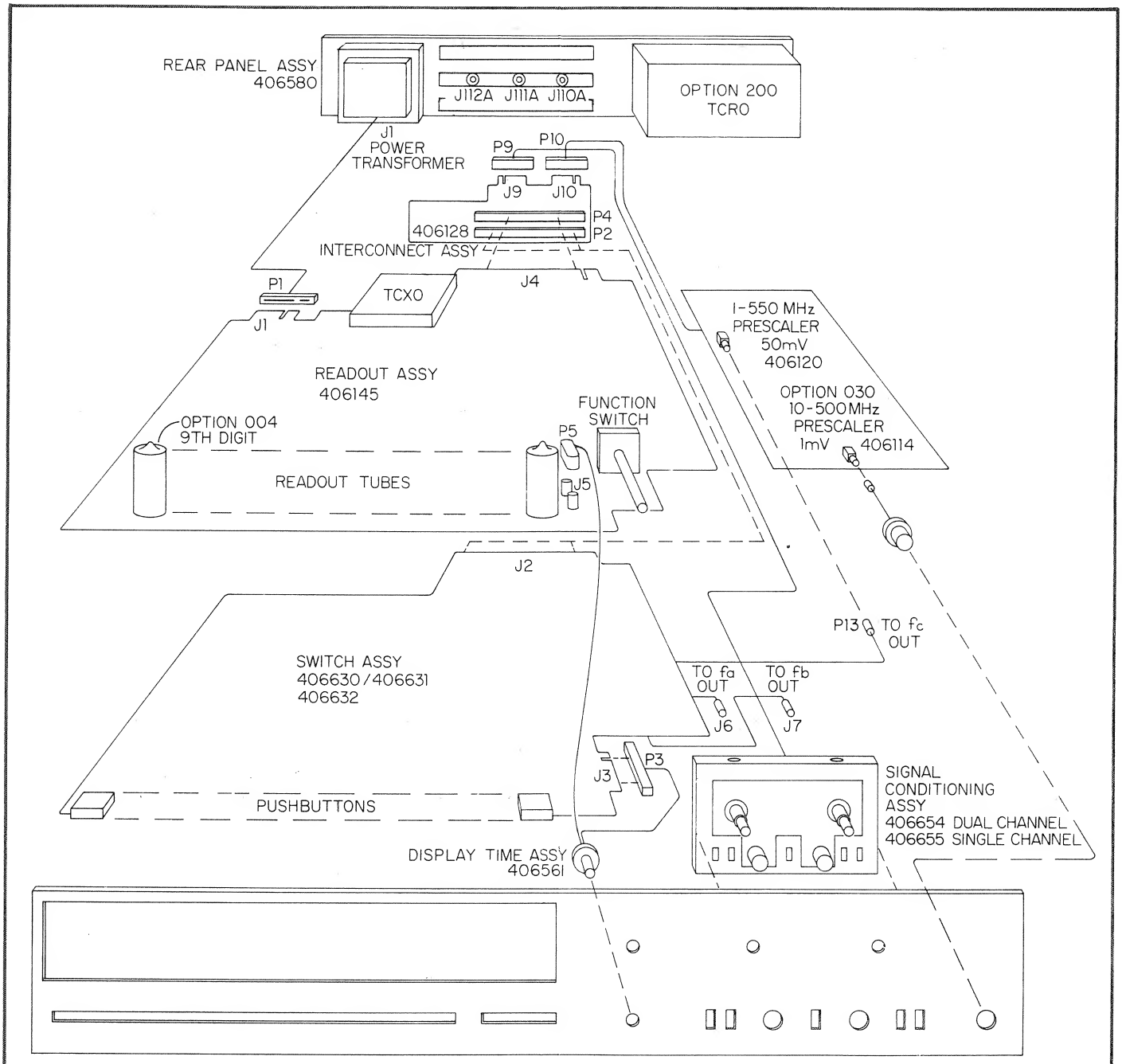
Table 5.9 - DC Levels

	TTL Gate High		TTL Gate Low	
V Source Output	3.4	4.2	3.4	4.2
V Load Input	3.4	4.2	3.14	3.14

5.113 BOARD REVISION.

5.114 Every effort is made to keep the manual concurrent with the instrument despite changes to the design, which are an inevitable adjunct of the manufacturing process. The manual is updated and periodically reprinted throughout the year. In between printings, Addendums and Errata Sheets are added to the manual if required to implement the reprinted copy.

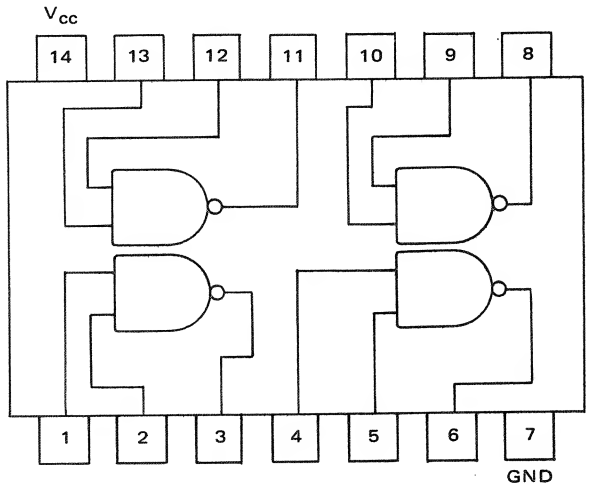
5.115 Any design change is accompanied by an updating of a board revision. Such change could be as simple as a revised hole size or as complex as major modifications of the circuitry. The revision of a board is indicated by the letter preceding the assembly number stamped on the board; the revision of the assembly drawing in Section 6 or on an Errata Sheet is indicated by the letter following the assembly number, located below the drawing. Comparing the revision letters can indicate how closely the drawing corresponds to the board.



ASSEMBLY NAME	MODEL	
	8010B	8030B
SIGNAL CONDITIONING	406654	406654
SWITCH BOARD	406631	406632
READOUT BOARD	406145	406145
REAR PANEL	406580	406580
550 MHz PRESCALER	NOTE ONLY 1 PRESCALER PER COUNTER	406120
500 MHz PRESCALER OPTION 030		406114
DISPLAY TIME CONTROL	406561	406561
INTERCONNECT BOARD	406128	406128
FRONT PANEL	730552	730555

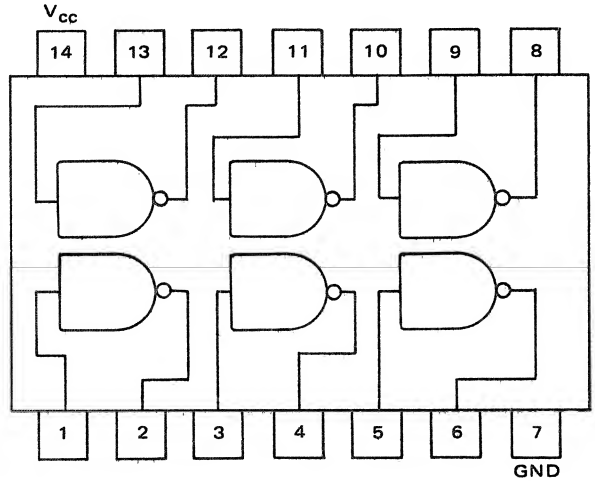
Figure 5.23 - Exploded View

7400 / 74H00
QUADRUPLE 2-INPUT POSITIVE NAND GATE



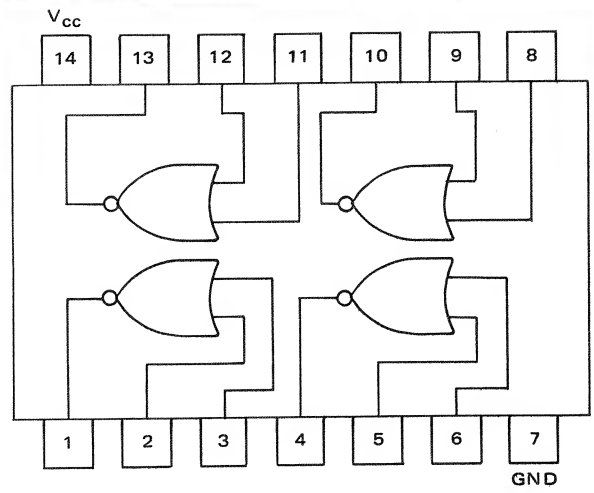
A	B	C
1	1	0
0	1	1
1	0	1
0	0	1

7404
HEX INVERTER



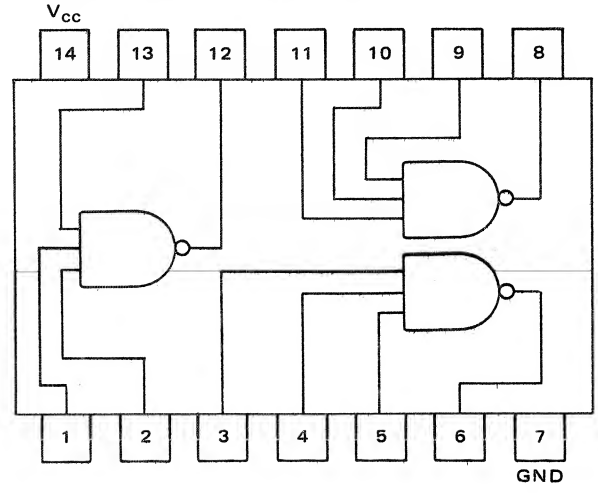
A	B
1	0
0	1

7402
QUADRUPLE 2-INPUT POSITIVE NOR GATE



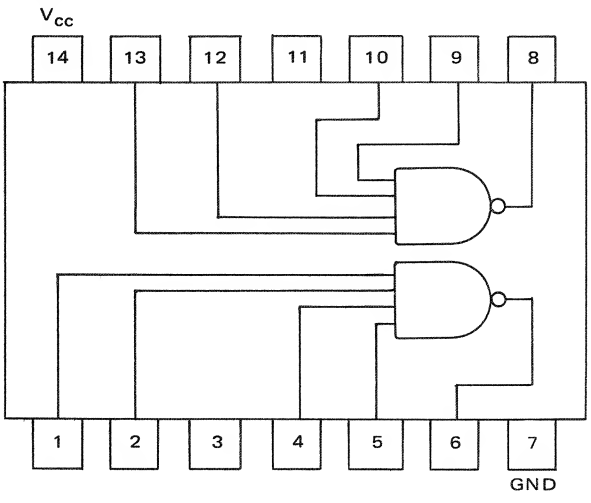
A	B	C
0	0	1
1	1	0
1	0	0
0	1	0

7410
TRIPLE 3-INPUT POSITIVE NAND GATE



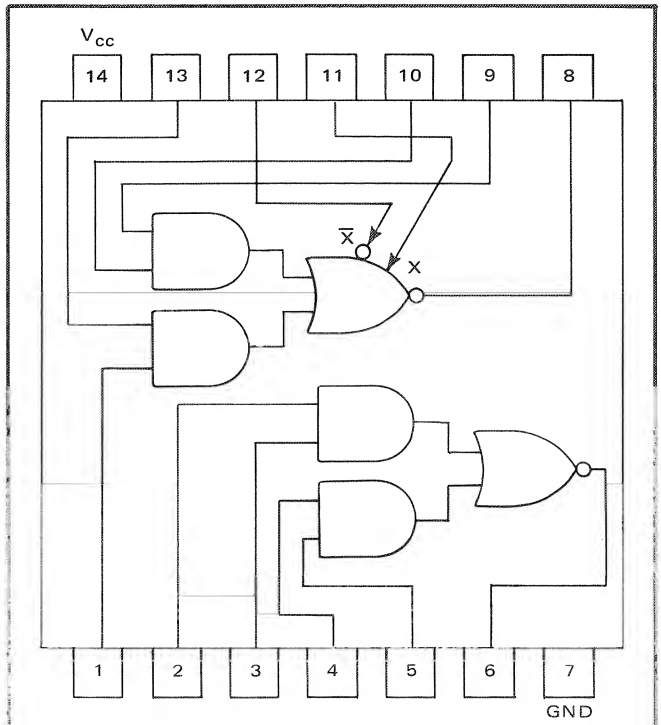
A	B	C	D
1	1	1	0
1	1	0	1
1	0	0	1
0	0	0	1

7420
DUAL 4-INPUT POSITIVE NAND GATE

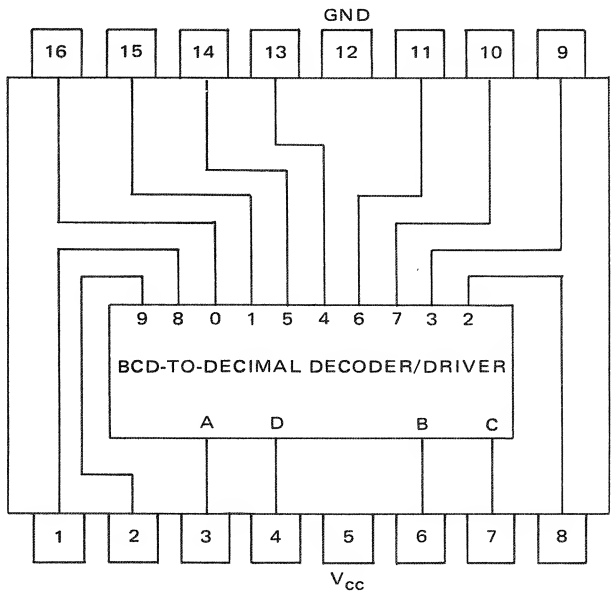


A	B	C	D	E
1	1	1	1	0
1	1	1	0	1
1	1	0	0	1
1	0	0	0	1
0	0	0	0	1

7451
EXPANDABLE DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



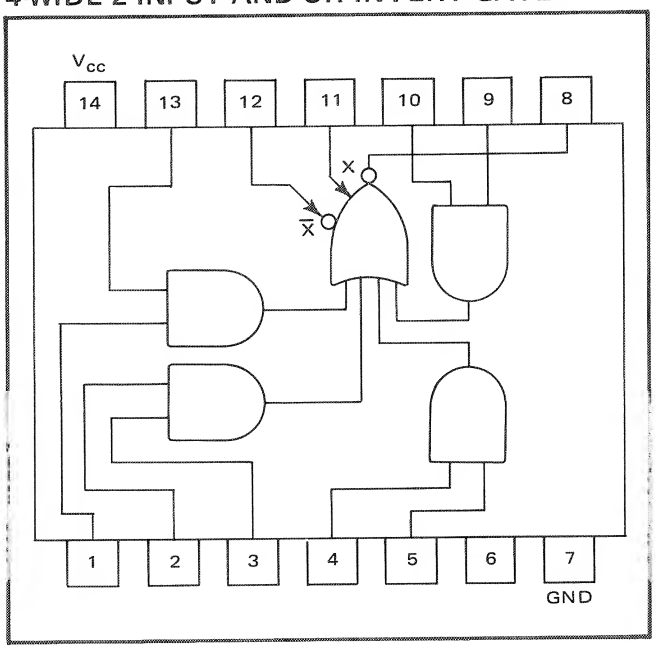
7441
BCD-TO-DECIMAL DECODER/DRIVER



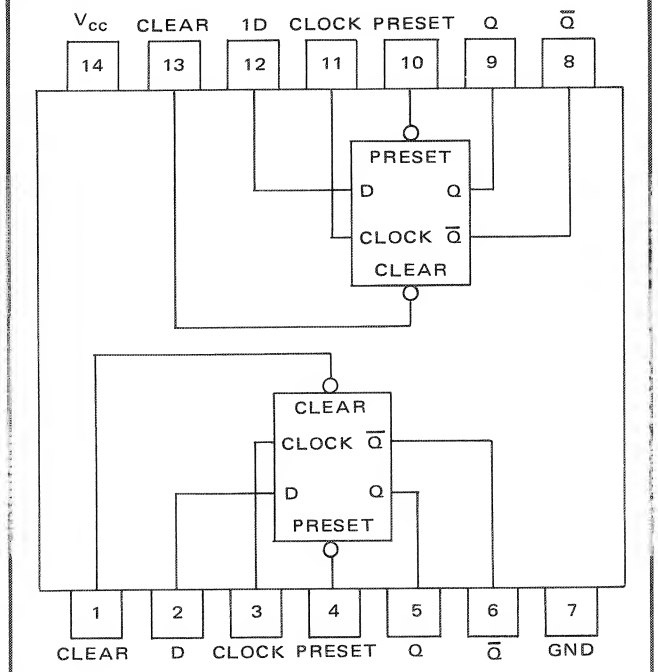
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

Figure 5.24 - Integrated Circuits

7454
4-WIDE 2-INPUT AND-OR-INVERT GATE



74H74
DUAL D-TYPE EDGE TRIGGERED FLIP-FLOP



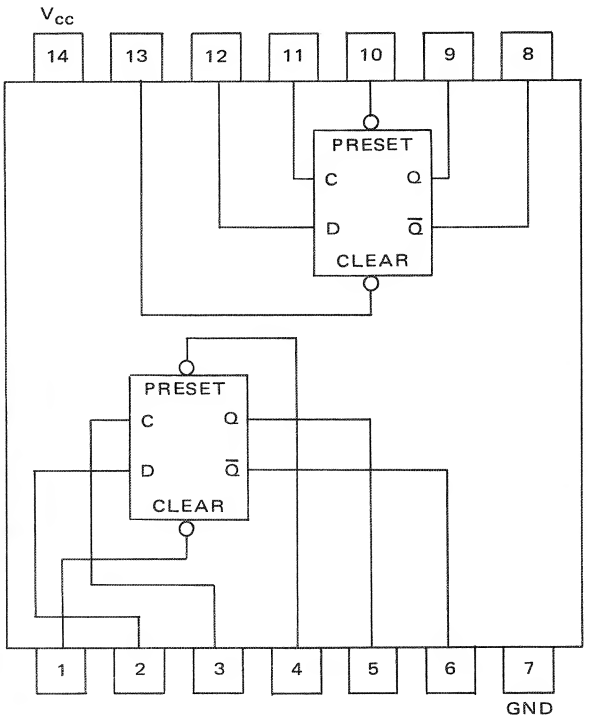
(Each Flip-Flop)		
t_n	t_{n+1}	
Input	Output	Output
D	Q	Q
L	L	H
H	H	L

H = High Level, L = Low Level

NOTES:

1. t_n = bit time before clock pulse
2. t_{n+1} = bit time after clock pulse

7474
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



D_n	Q_{n+1}	$\bar{Q}_{n+1}$
1	1	0
0	0	1

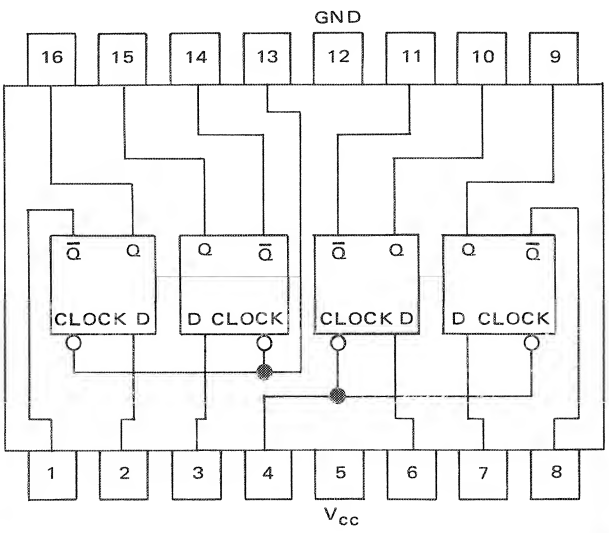
Preset	Clear	Q
1	1	Q
1	0	0
0	1	1
0	0	†

† Both outputs in 1 state

n is time prior to clock

n + 1 is time following clock

7475
QUADRUPLE BISTABLE LATCH

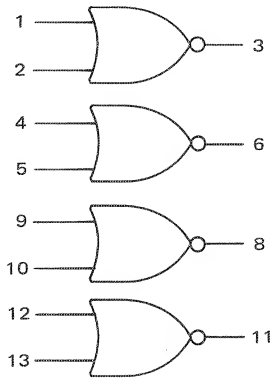


(Each Latch)		
t_n	t_{n+1}	
D	Q	$\bar{Q}$
1	1	0
0	0	1

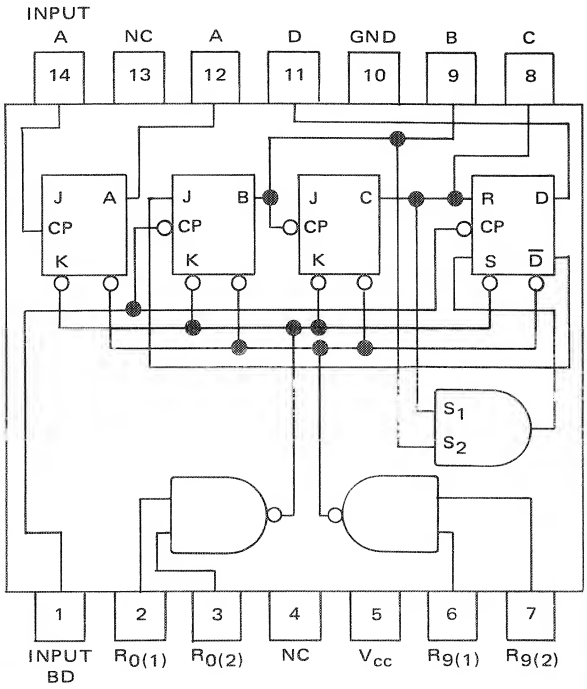
NOTES:

1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.
3. These voltages are with respect to network ground terminal.

MC1010
QUAD 2-INPUT GATES



7490
DECADE COUNTER



BCD COUNT SEQUENCE (See Note 1)

	OUTPUT			
COUNT	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

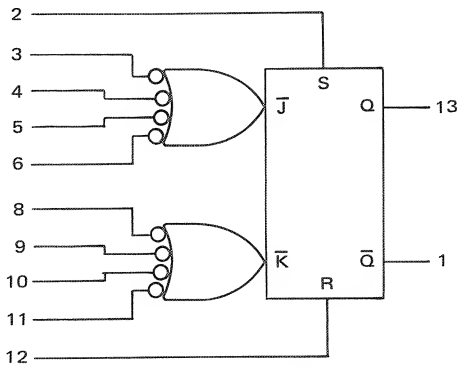
RESET INPUTS				OUTPUT			
$R_{0(2)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

NOTES:

1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 of a logical 0 may be present.
3. Fanout from output A to input BD and to 10 additional Series 54/74 loads is permitted.

Figure 5.24 - Integrated Circuits continued

MC1013 / MC1027
AC-COUPLED J-K FLIP-FLOP



MC1013
DC Input Loading Factor = 1
DC Output Loading Factor = 25
tpd = 6.0 ns typ
Power Dissipation = 125 mW typ

MC1027
DC Input Loading Factor = 2
DC Output Loading Factor = 25
tpd = 4.0 ns typ
Power Dissipation = 250 mW typ

R-S TRUTH TABLE

	R	S	Q^{n+1}
Pin No.	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ inputs are static.
N.D. = Not defined.

$\overline{J}_D$ - $\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$	$\overline{K}_D$	Q^{n+1}
	*	*	13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

Pin No.	$\overline{J}$	$\overline{K}$	$\overline{C}_D$	Q^n
	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

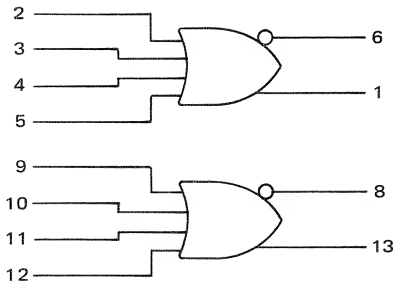
All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

* Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.

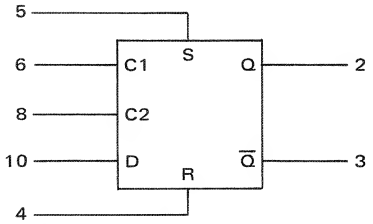
** $\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} – 0.6V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

MC1023
DUAL 4-INPUT CLOCK DRIVER



MC1034
TYPE D FLIP-FLOP



DC Input Loading Factor:
C = 1, D = 2, R and S = 6
DC Output Loading Factor = 25
Power Dissipation = 185 mW typical using external 600-ohm pull-down resistors
240 mW typical using internal pull-down resistors

R-S TRUTH TABLE

	R	S	Q^{n+1}	$\overline{Q}^{n+1}$
Pin No.	4	5	2	3
	0	0	Q^n	$\overline{Q}^n$
	0	1	1	0
	1	0	0	1
	1	1	N.D.	N.D.

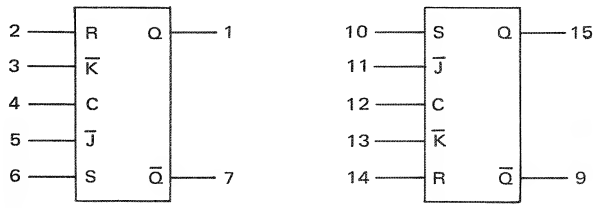
N.D. = Not Defined

CLOCKED TRUTH TABLE

	D	C	Q^{n+1}	$\overline{Q}^{n+1}$
Pin No.	10	6 or 8	2	3
	0	0	Q^n	$\overline{Q}^n$
	1	0	Q^n	$\overline{Q}^n$
	0	1*	0	1
	1	1*	1	0

*A "1" or Clock input is defined for this flip-flop as a change in level from a low state to a high state of the clock.

MC1032
100-MHz AC-COUPLED DUAL J-K FLIP-FLOP



V_{CC} = Pin 16
V_{EE} = Pin 8

DC Input Loading Factor:
Clock = 2
$\overline{J}$, $\overline{K}$, S, R = 1
DC Output Loading Factor = 25
tpd = 4.5 ns typ
Power Dissipation = 180 mW typ

R-S TRUTH TABLE

Pin No.	R	S	Q^{n+1}
	2 & 14	6 & 10	1 & 15
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D.

All $\overline{J}$-$\overline{K}$ inputs and Clock inputs are static
N.D. = Not defined

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}$	$\overline{K}$	Q^{n+1}
	*	*	1 & 15
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Clock inputs and the R-S inputs are at a "0" level.

CLOCKED $\overline{J}$-$\overline{K}$ TRUTH TABLE

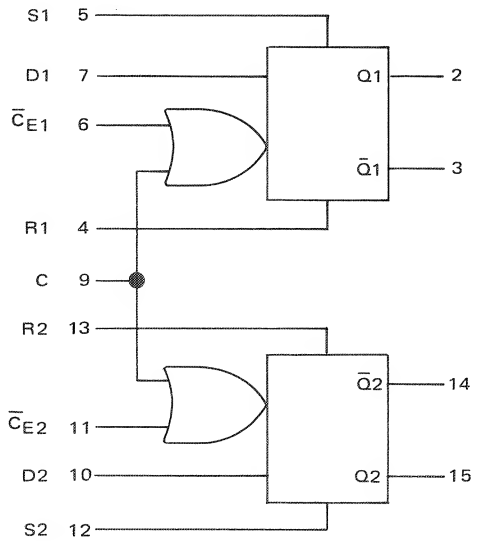
Pin No.	$\overline{J}$	$\overline{K}$	Clock	Q^n
	*	*	4 & 12	1 & 15
	Ø	Ø	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All other $\overline{J}$-$\overline{K}$ inputs and the R-S inputs are at a "0" level.
Ø = Either state will result in the desired output.

* Any $\overline{J}$ or $\overline{K}$ input

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the clock input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logic "1" only while the clock input is in a logic "1" state. (Clock maximum "1" level = V_{CC} – 0.7V.)

MC10131
DUAL TYPE D MASTER-SLAVE FLIP-FLOP



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

R-S TRUTH TABLE

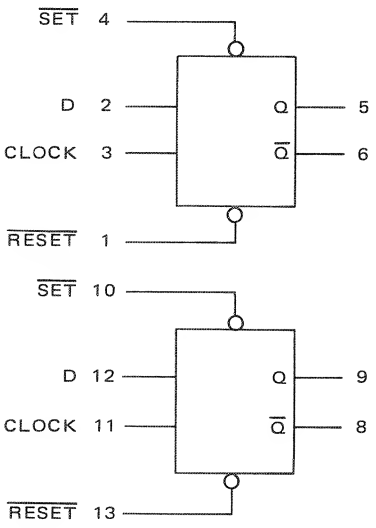
R	S	Q^{n+1}	$\overline{Q}^{n+1}$
L	L	Q^n	$\overline{Q}^n$
L	H	H	L
H	L	L	H
H	H	N.D.	N.D.

N.D. = Not Defined

SEQUENTIAL TRUTH TABLE

D	C	$\overline{C}_E$	Q_{n+1}
L	L	L	Q_n
L	L	H	L
L	H	L	Q_n
L	H	H	Q_n
H	L	L	Q_n
H	L	H	H
H	H	L	Q_n
H	H	H	Q_n

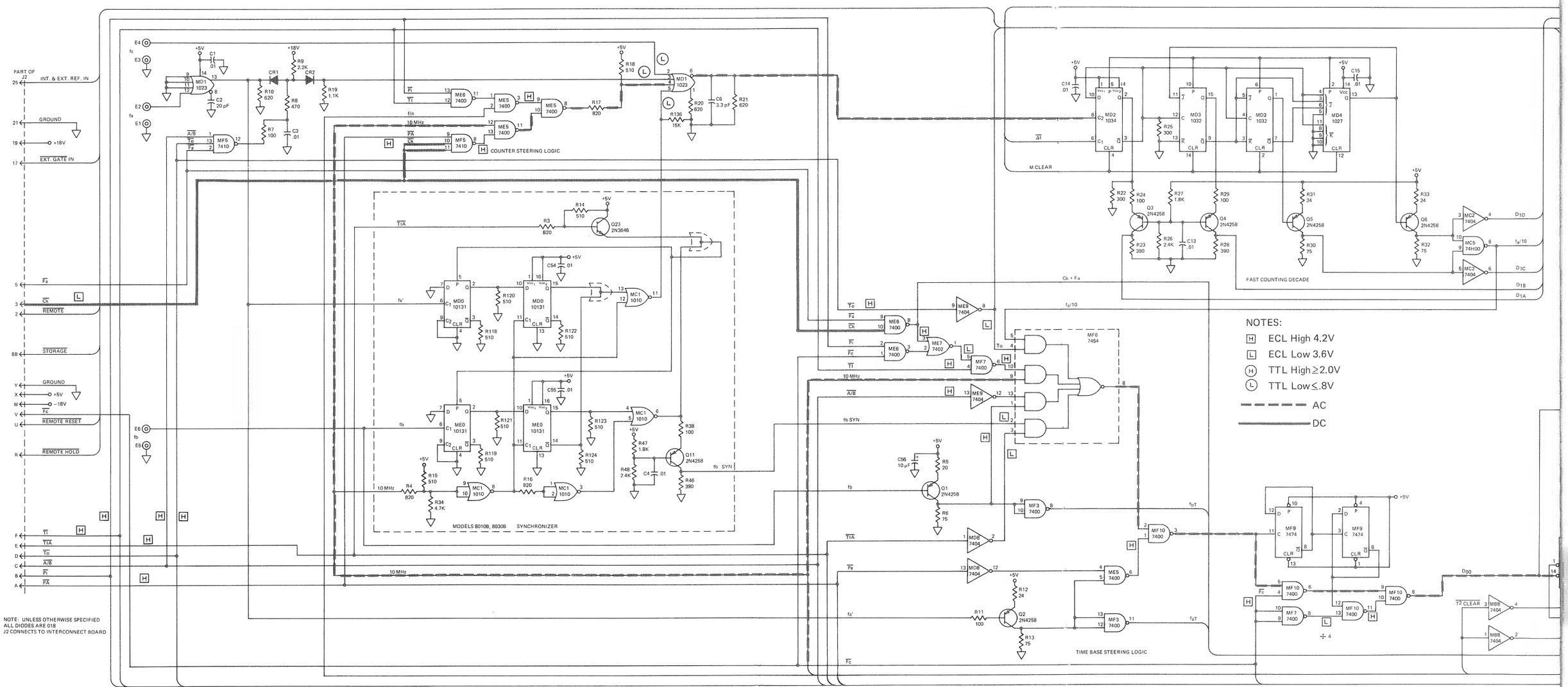
DUAL TYPE D FLIP-FLOP MC3060F

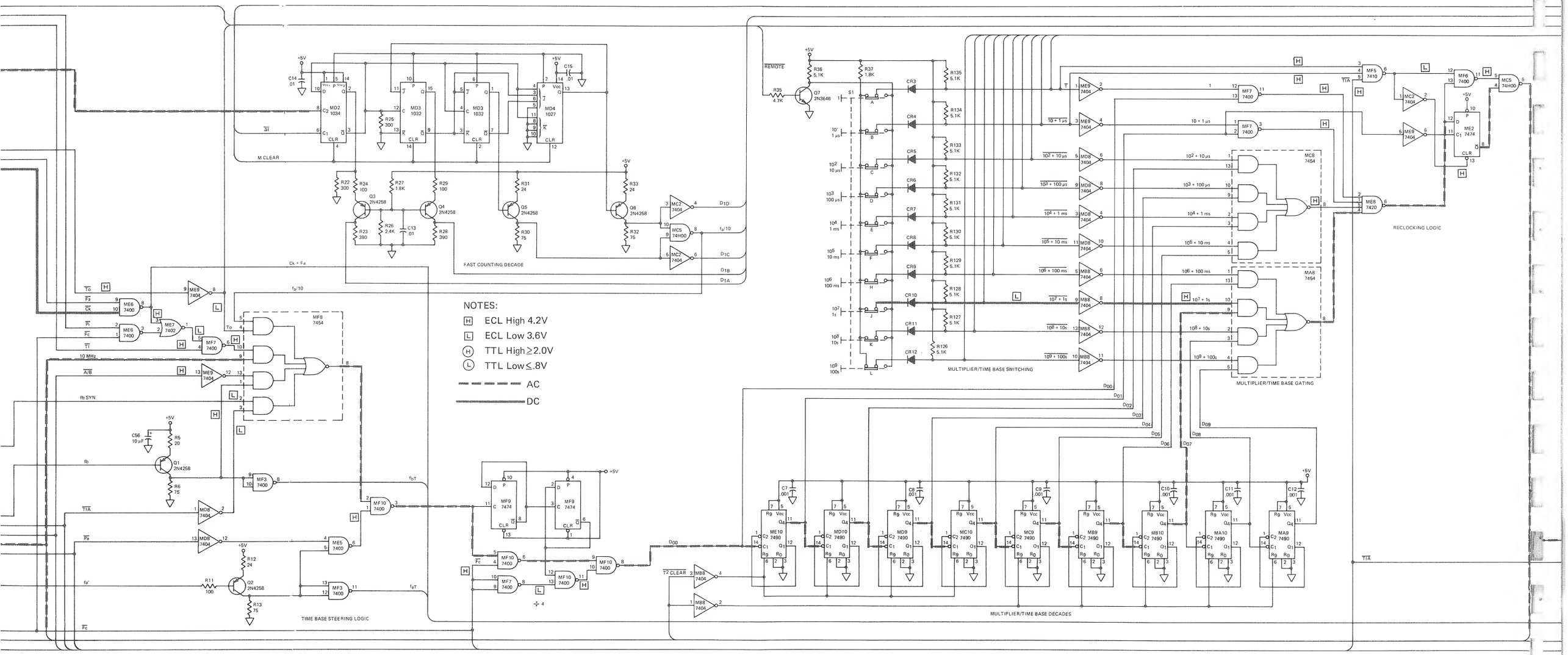


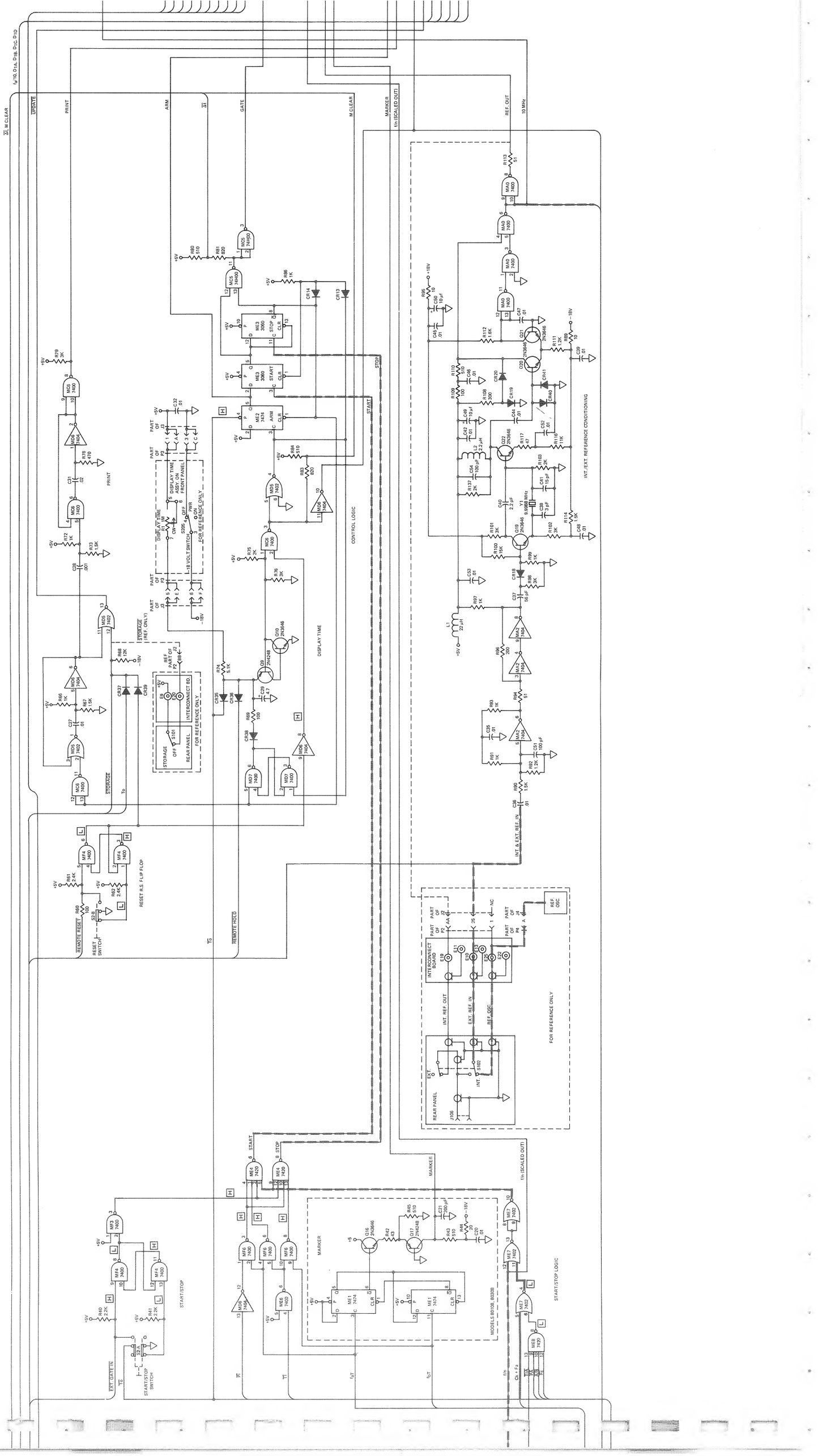
TRUTH TABLE

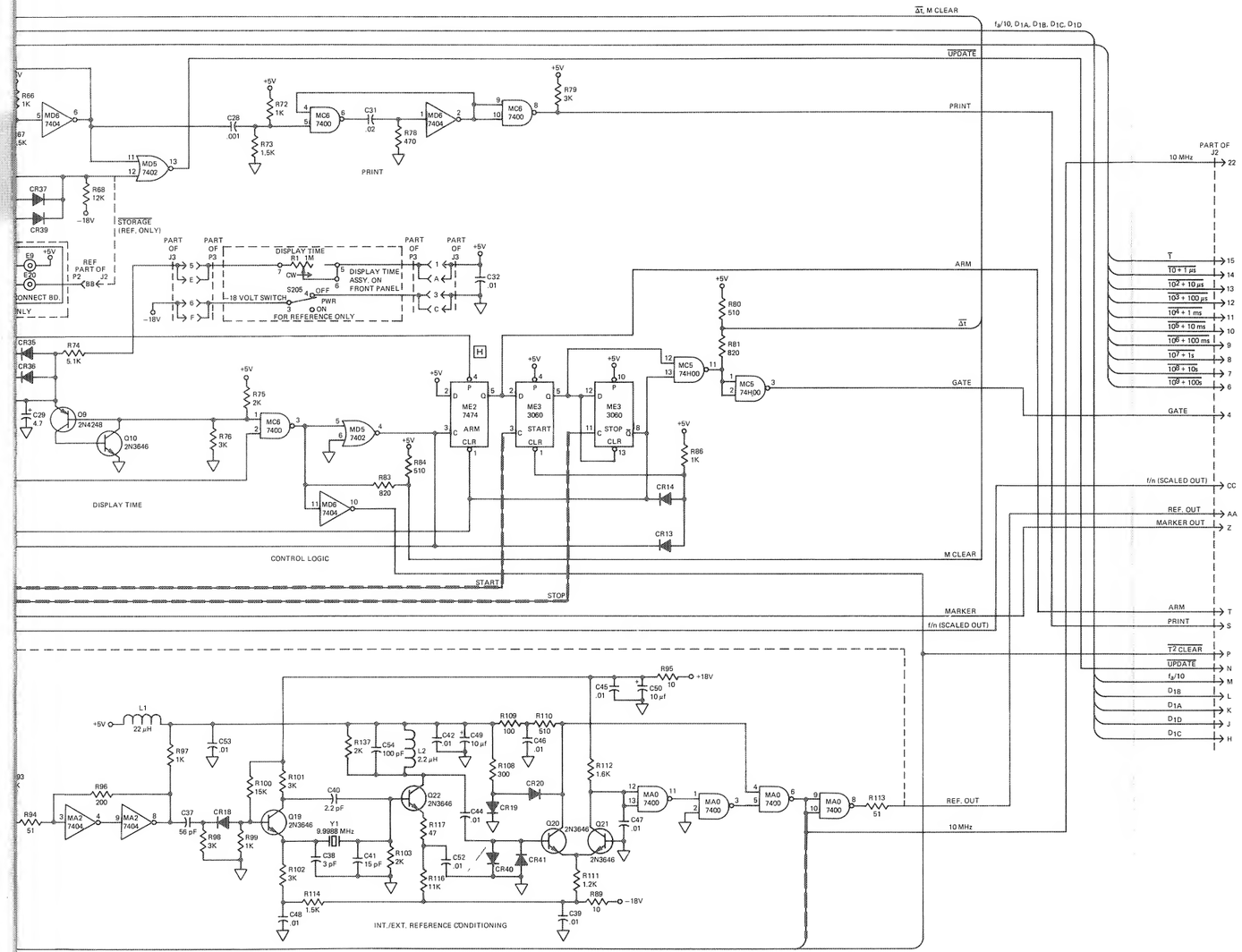
D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

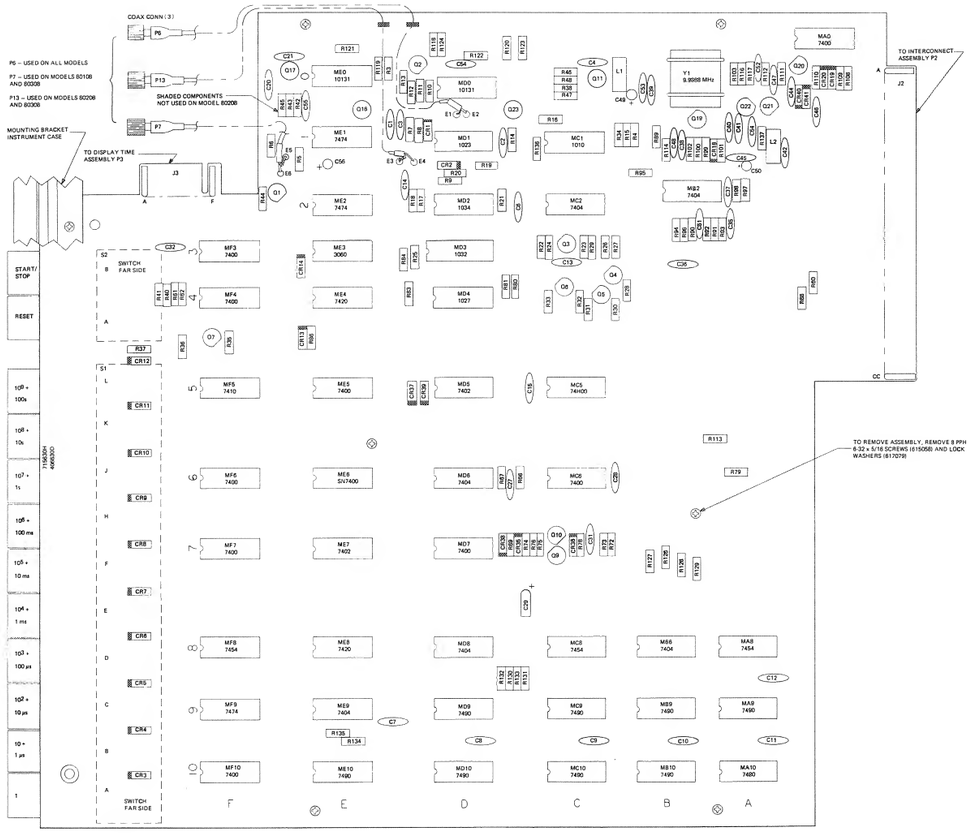
$Q^{n+1} = D^n$

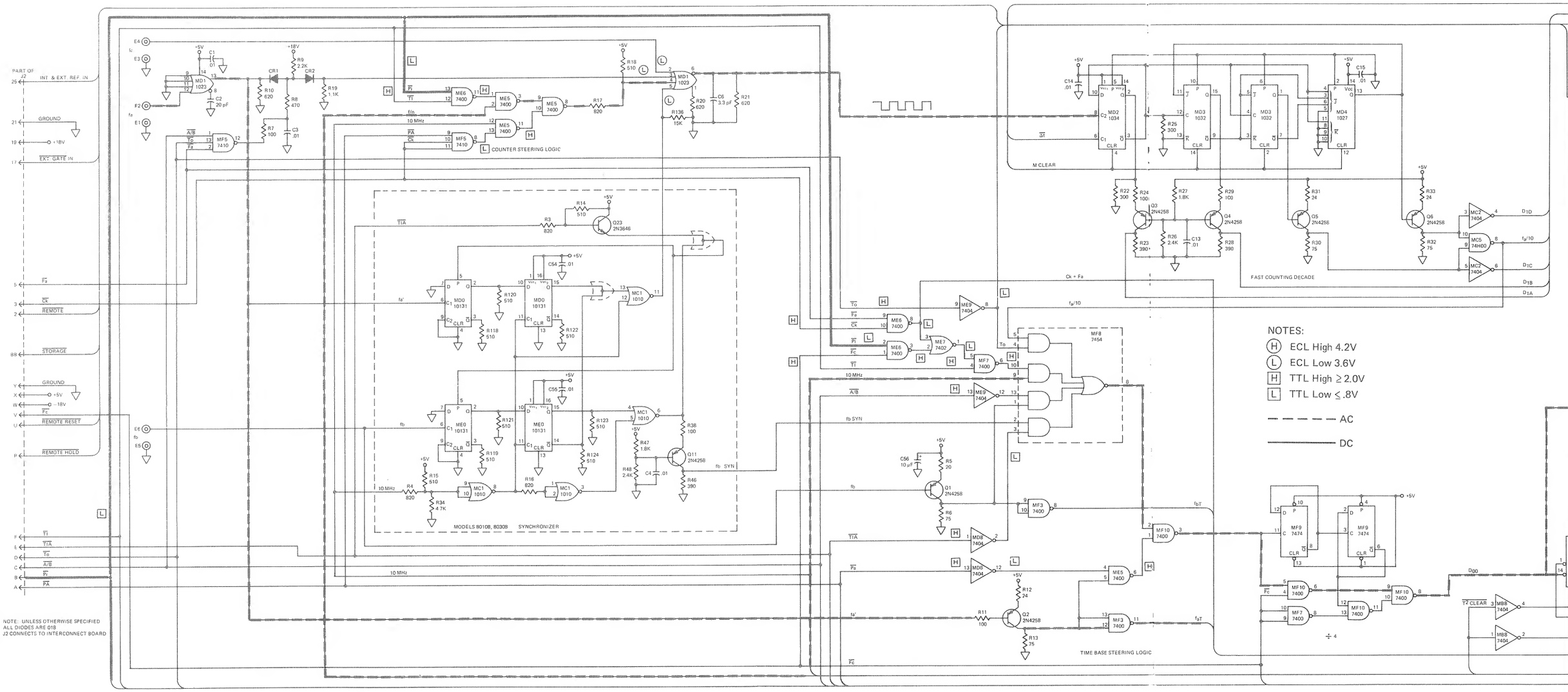

PART OF J2
INT. & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
REMOTE
STORAGE
GROUND
+5V
−18V
REMOTE RESET
REMOTE HOLD
COUNTER STEERING LOGIC
MODELS 8010B, 8030B SYNCHRONIZER
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥2.0V
L TTL Low ≤.8V
AC
DC
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 01B
J2 CONNECTS TO INTERCONNECT BOARD

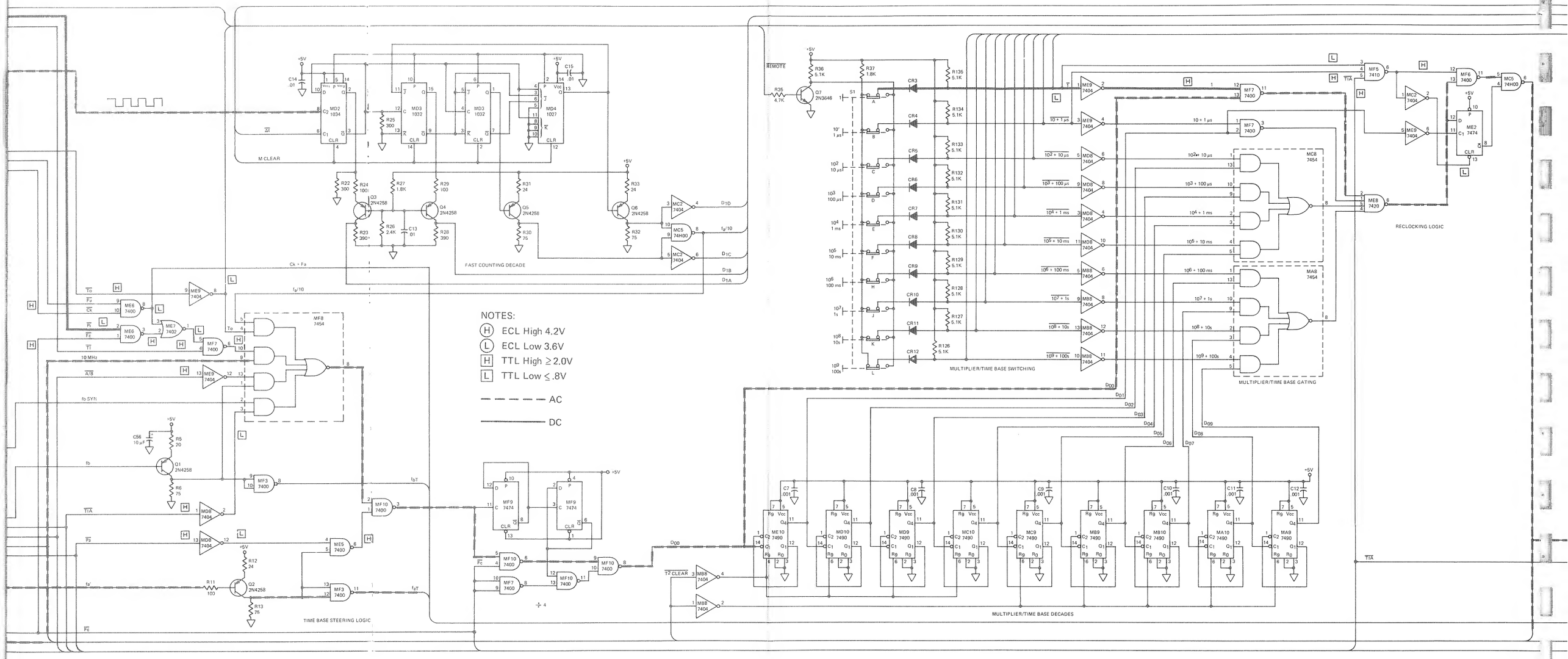

REMOTE
R36 5.1K
R37 1.8K
R35 4.7K
Q7 2N3646
S1
CR3
CR4
CR5
CR6
CR7
CR8
CR9
CR10
CR11
CR12
R135 5.1K
R134 5.1K
R133 5.1K
R132 5.1K
R131 5.1K
R130 5.1K
R129 5.1K
R128 5.1K
R127 5.1K
R126 5.1K
MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
RECLOCKING LOGIC
MD2 1034
MD3 1032
MD4 1027
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
MULTIPLIER/TIME BASE DECADES
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
(H) TTL High ≥2.0V
(L) TTL Low ≤.8V
AC
DC


UPDATE
PRINT
ARM
GATE
M CLEAR
MARKER
REF. OUT
10 MHz
STOP
START
CONTROL LOGIC
DISPLAY TIME
STORAGE
REMOTE HOLD
REMOTE RESET
RESET R.S. FLIP FLOP
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
FOR REFERENCE ONLY
START/STOP LOGIC
MODELS 80108, 80208
EXT. GATE IN
START/STOP SWITCH
REAR PANEL
INTERCONNECT BOARD
REF OSC
INT. REF. OUT
EXT. REF. IN
REF. OSC
1-18 VOLT SWITCH
DISPLAY TIME ASSY. ON FRONT PANEL
STORAGE (REF. ONLY)
INTERCONNECT BD.

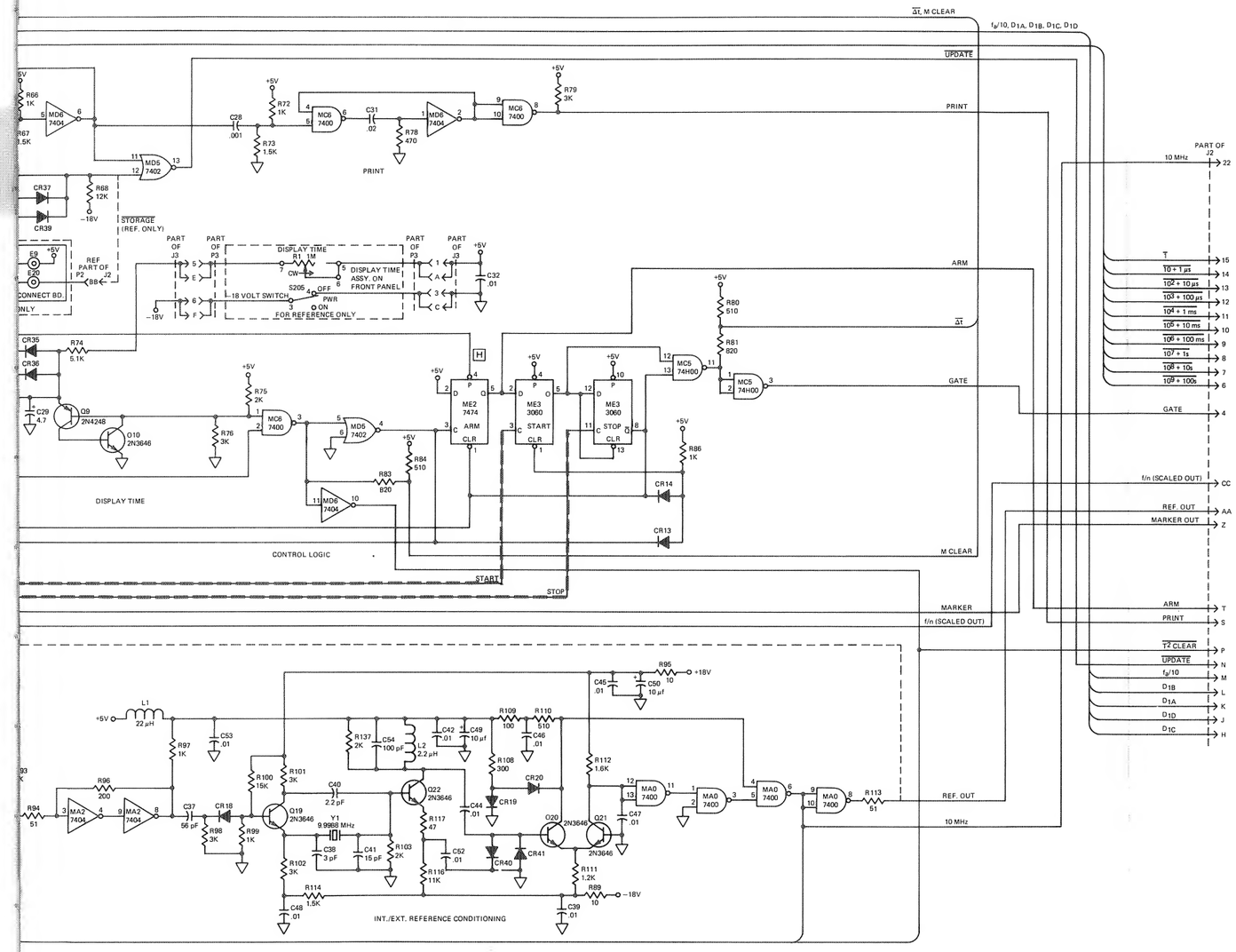

ΔT, M CLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
ΔT
GATE
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
REF. OUT
10 MHz
PART OF J2
22
T
15
10⁰ + 1 µs
14
10² + 10 µs
13
10³ + 100 µs
12
10⁴ + 1 ms
11
10⁵ + 10 ms
10
10⁶ + 100 ms
9
10⁷ + 1s
8
10⁸ + 10s
7
10⁹ + 100s
6
GATE
4
f/n (SCALED OUT)
CC
REF. OUT
AA
MARKER OUT
Z
ARM
T
PRINT
S
T2 CLEAR
P
UPDATE
N
f0/10
M
D1B
L
D1A
K
D1D
J
D1C
H
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
REF PART OF P2
PART OF P3
PART OF J3
DISPLAY TIME R1 1M
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
S205
PWR ON OFF
FOR REFERENCE ONLY
CONNECT BD
ONLY
ME2 7474 ARM CLR
ME3 3060 START CLR
ME3 3060 STOP CLR
MC5 74H00
MC6 7400
MD5 7402
MD6 7404
MA2 7404
MA0 7400
Q9 2N4248
Q10 2N3646
Q19 2N3646
Q20 2N3646
Q21 2N3646
Q22 2N3646
Y1 9.9988 MHz
L1 22 µH
L2 2.2 µH
+5V
-18V
+18V

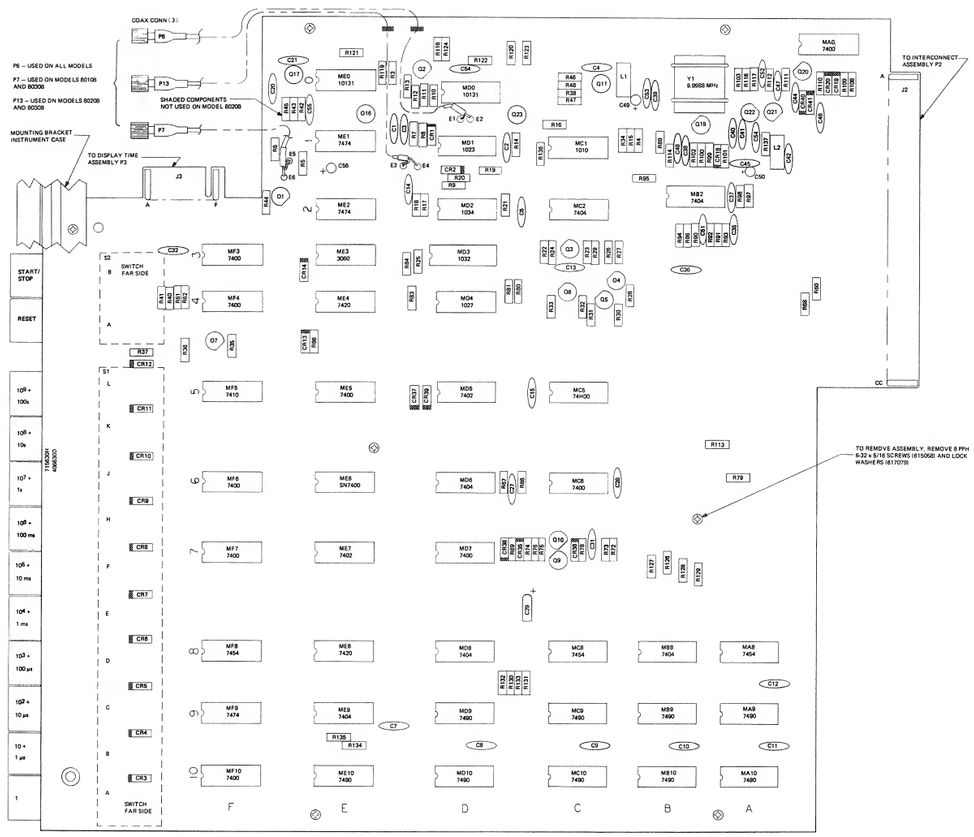

COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 60108 AND 60308
P13 – USED ON MODELS 60208 AND 60308
SHADED COMPONENTS NOT USED ON MODEL 60208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6190568) AND LOCK WASHERS (6170791)
START/ STOP
RESET
SWITCH FAR SIDE
Y1 9.9988 MHz
MA0 7400
MB2 7404
MC1 1010
MC2 7404
MD1 1023
MD2 1034
MD3 1032
MD4 1027
ME0 10131
ME1 7474
ME2 7474
ME3 3060
ME4 7420
MF3 7400
MF4 7400
MF5 7410
ME5 7400
MD5 7402
MC5 74H00
MF6 7400
ME6 SN7400
MD6 7404
MC6 7400
MF7 7400
ME7 7402
MD7 7400
MF8 7454
ME8 7420
MD8 7404
MC8 7454
MB6 7404
MA8 7454
MF9 7474
ME9 7404
MD9 7490
MC9 7490
MB9 7490
MA9 7490
MF10 7400
ME10 7490
MD10 7490
MC10 7490
MB10 7490
MA10 7480
SWITCH FAR SIDE

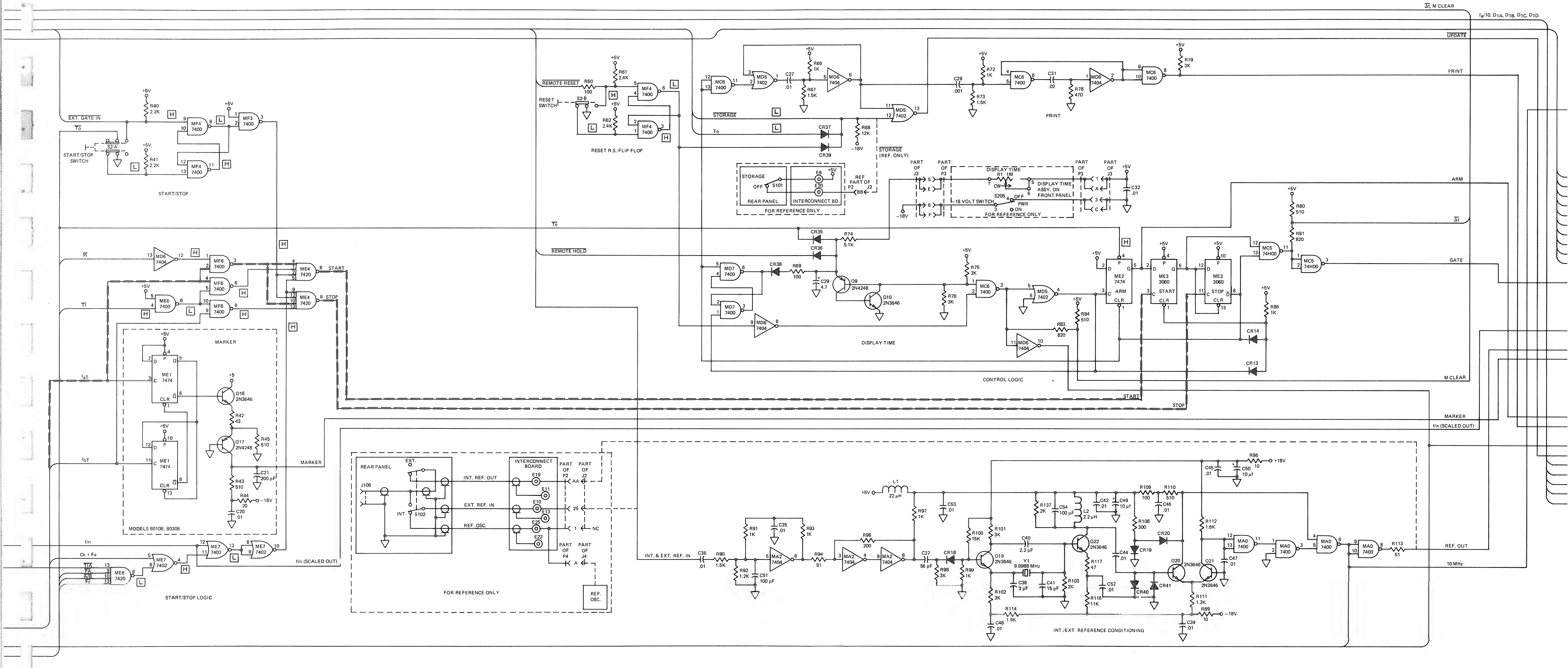

PART OF J2
INT & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
GROUND
+5V
-18V
REMOTE RESET
REMOTE HOLD
STORAGE
REMOTE
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE D1B
J2 CONNECTS TO INTERCONNECT BOARD
COUNTER STEERING LOGIC
MODELS 8010B, 8030B SYNCHRONIZER
TIME BASE STEERING LOGIC
FAST COUNTING DECADE
M CLEAR
10 MHz
÷ 4
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC



5-22 Signal Flow for Period Mode


$\overline{\Delta t}$, M CLEAR
$f_B/10$, D_{1A}, D_{1B}, D_{1C}, D_{1D}
UPDATE
PRINT
ARM
$\overline{\Delta t}$
GATE
GATE
t/n (SCALED OUT)
REF. OUT
MARKER OUT
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
ARM
PRINT
$\overline{T2}$ CLEAR
UPDATE
$f_B/10$
D_{1B}
D_{1A}
D_{1D}
D_{1C}
REF. OUT
10 MHz
PART OF J2
T
10^{-1} + 1 µs
10^{2} + 10 µs
10^{3} + 100 µs
10^{4} + 1 ms
10^{5} + 10 ms
10^{6} + 100 ms
10^{7} + 1s
10^{8} + 10s
10^{9} + 100s
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
18 VOLT SWITCH
FOR REFERENCE ONLY
+5V
−18V
10 MHz

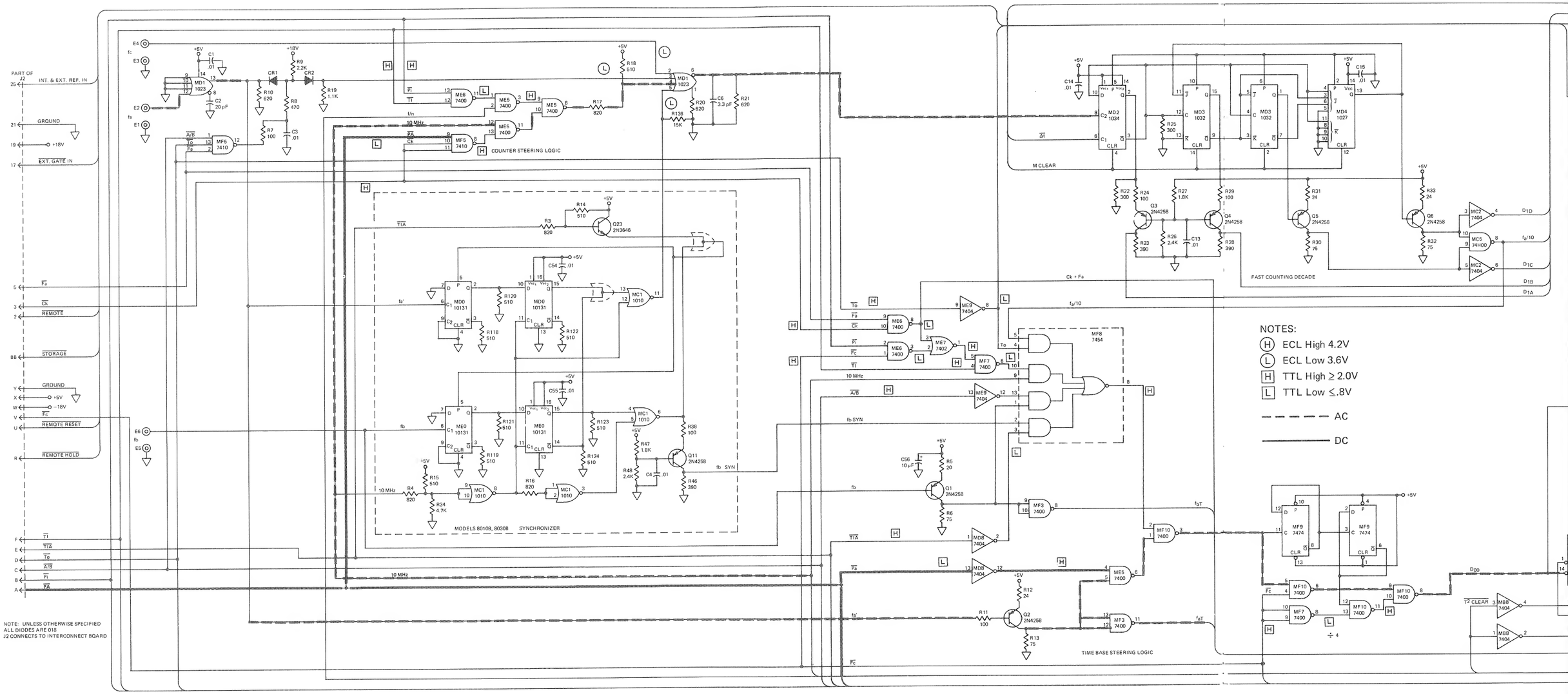

COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80308
P13 – USED ON MODELS 80208 AND 80308
SHADED COMPONENTS NOT USED ON MODEL 80208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6150568) AND LOCK WASHERS (6170709)
START/ STOP
RESET
SWITCH FAR SIDE
Y1 9.9988 MHz
F
E
D
C
B
A

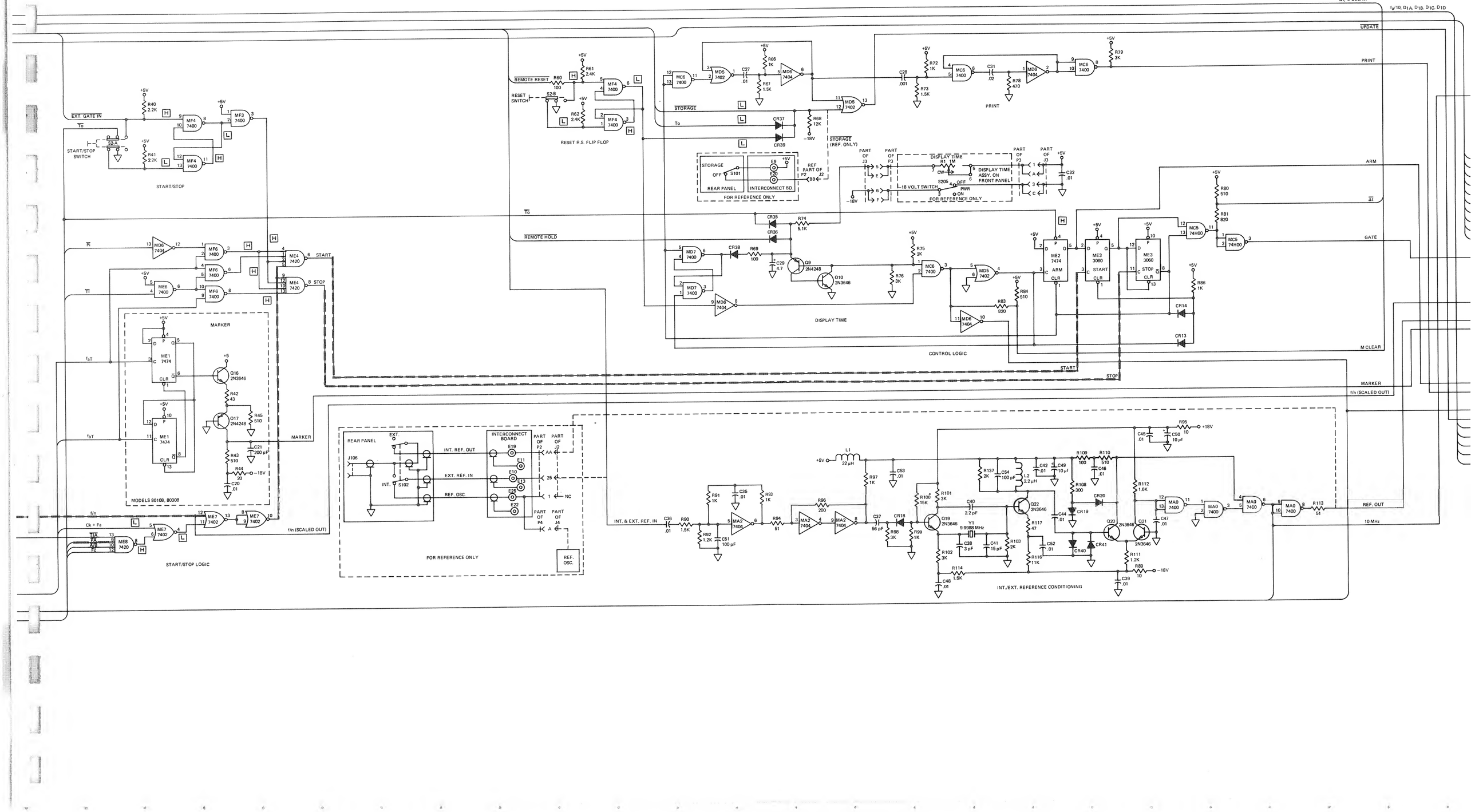


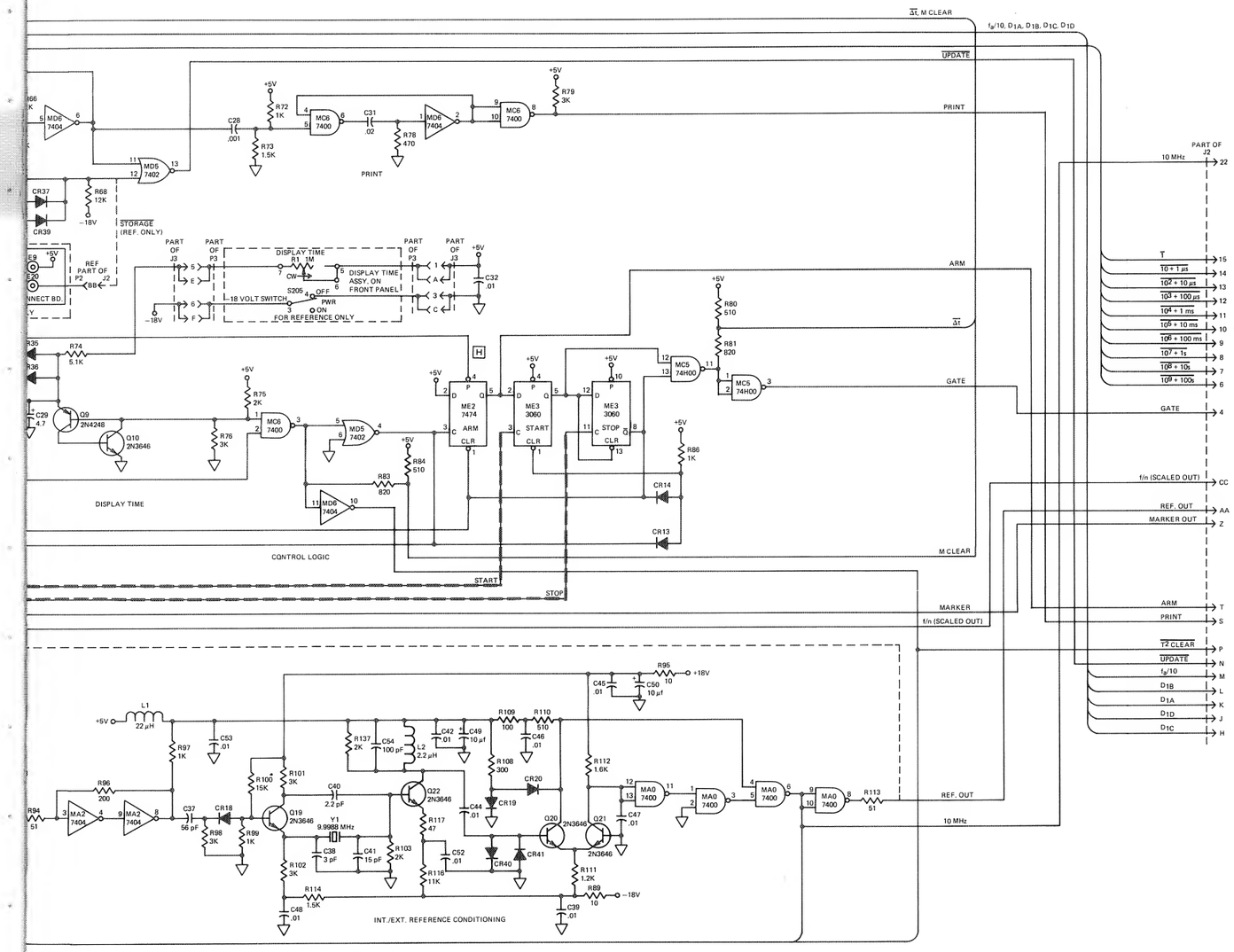
START/STOP
START/STOP SWITCH
RESET R.S. FLIP FLOP
REMOTE RESET
RESET SWITCH
STORAGE
PRINT
DISPLAY TIME
CONTROL LOGIC
MARKER
MODELS 8010B, 8030B
START/STOP LOGIC
FOR REFERENCE ONLY
REAR PANEL
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT./EXT. REFERENCE CONDITIONING
INT. & EXT. REF. IN
REF. OUT
10 MHz
M CLEAR
UPDATE
ARM
GATE
START
STOP
f/n (SCALED OUT)
REMOTE HOLD
DISPLAY TIME ASSY. ON FRONT PANEL
-18 VOLT SWITCH

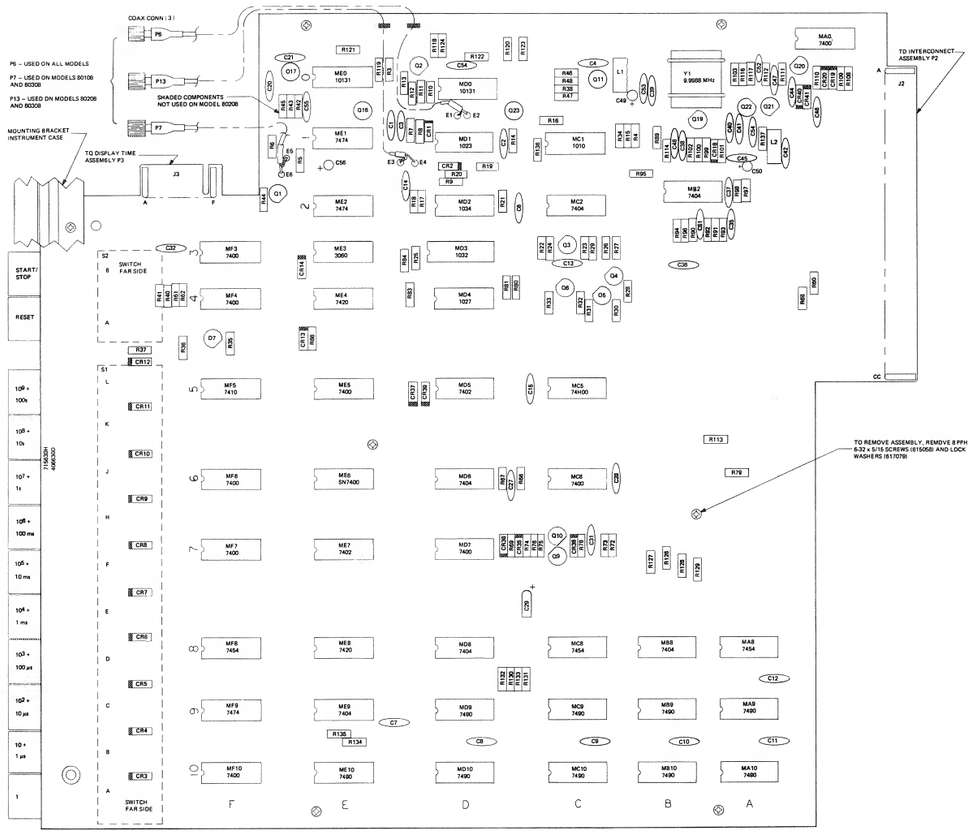
NOTES:
- (H) ECL High 4.2V
- (L) ECL Low 3.6V
- [H] TTL High ≥ 2.0V
- [L] TTL Low ≤.8V
- AC
- DC

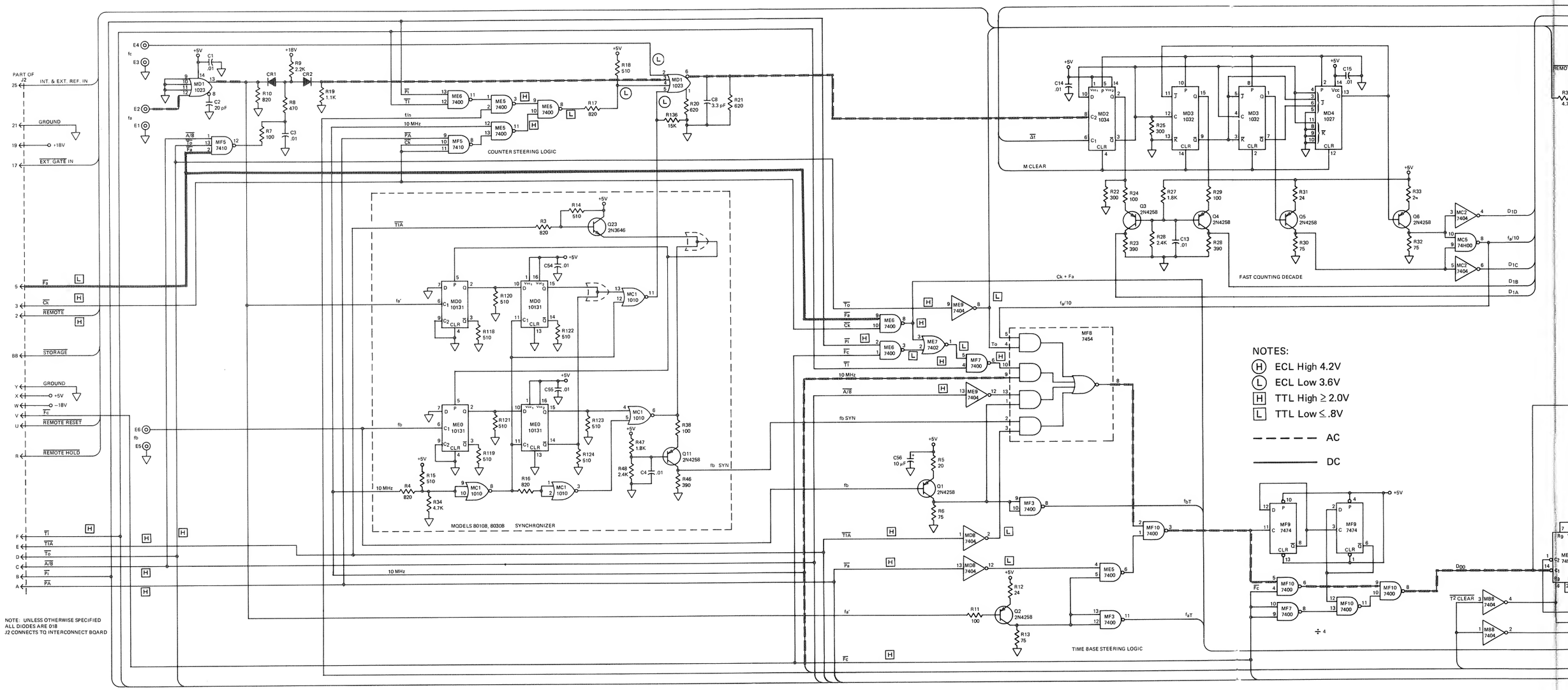
5-24 Signal Flow for Period Average Mode

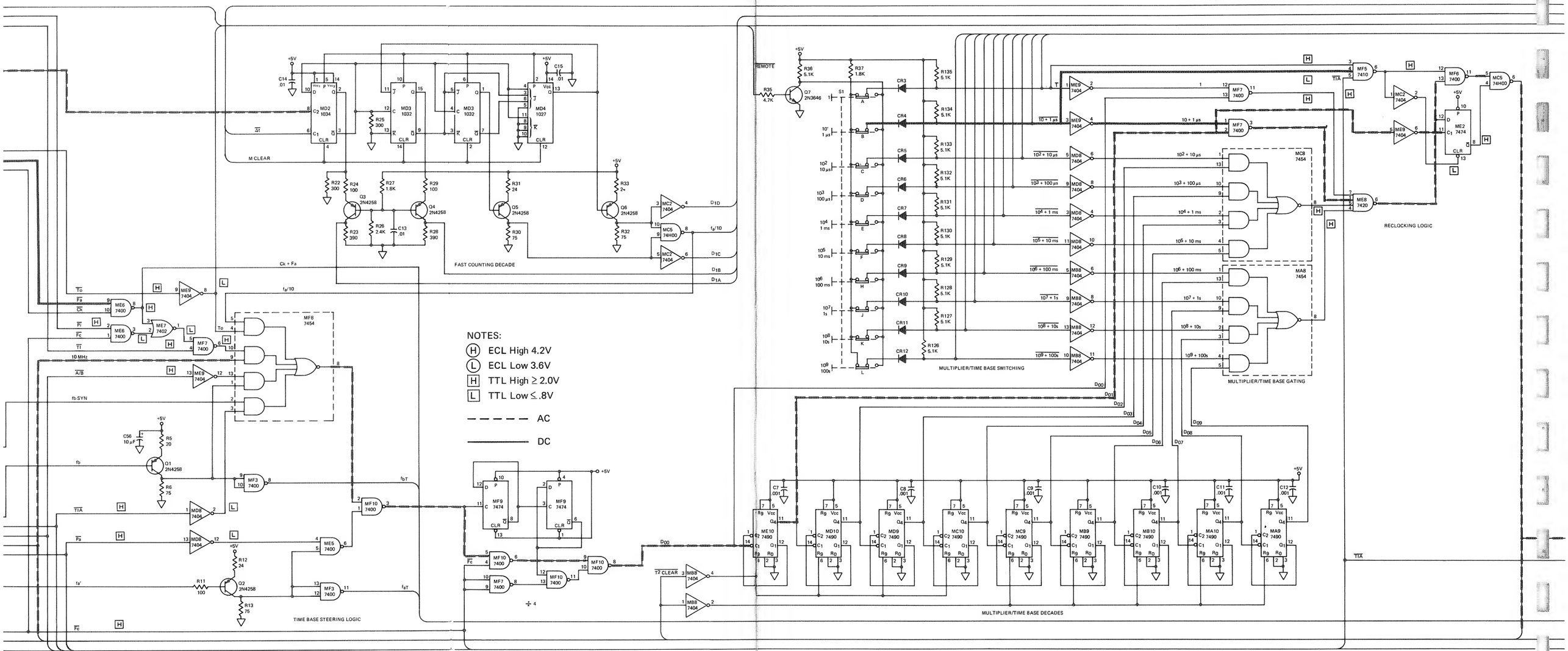

PART OF J2
INT. & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
GROUND
+5V
−18V
REMOTE RESET
REMOTE HOLD
STORAGE
REMOTE
COUNTER STEERING LOGIC
10 MHz
MODELS 80108, 80308 SYNCHRONIZER
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
÷ 4
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤.8V
AC
DC
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

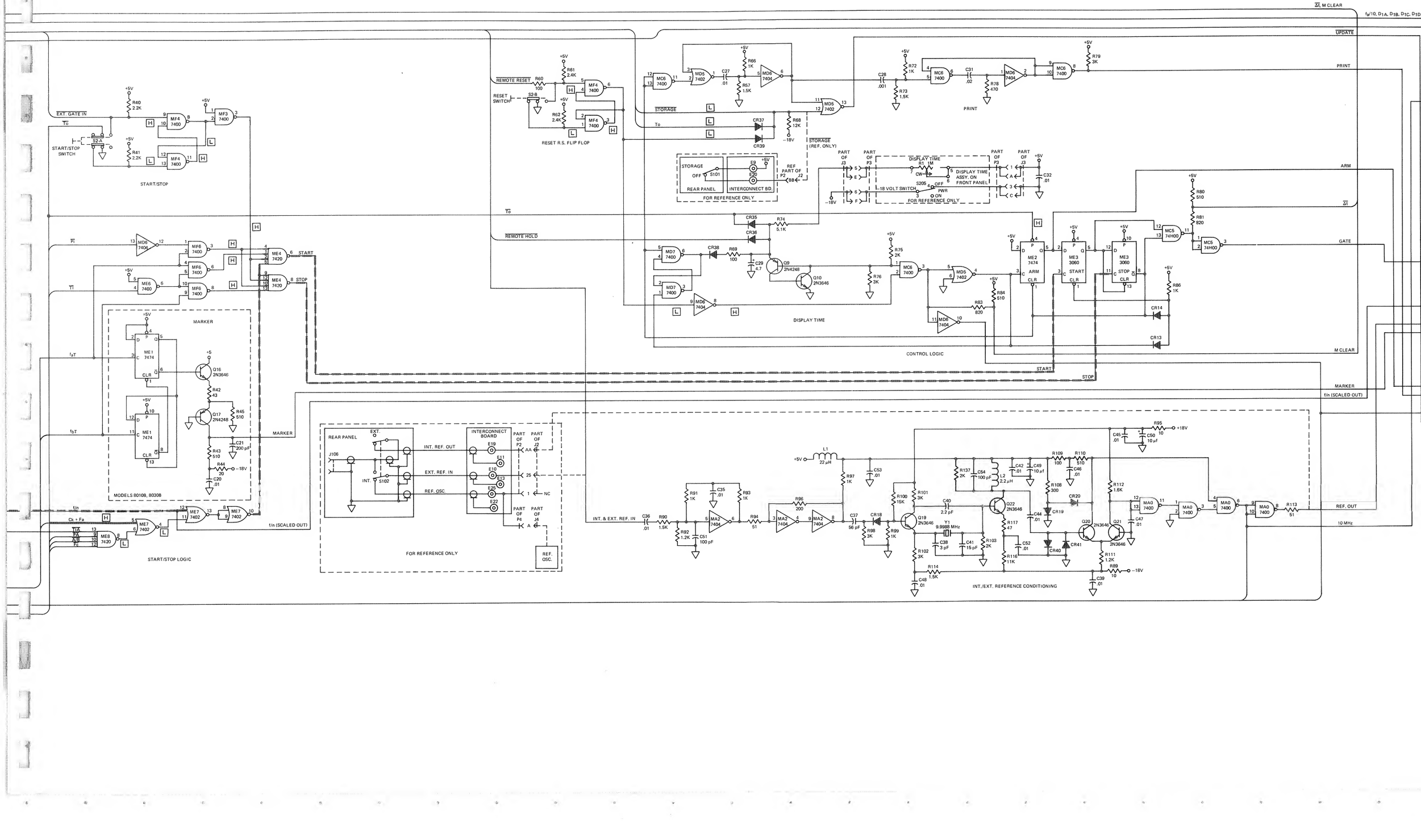

EXT. GATE IN
START/STOP SWITCH
START/STOP
RESET R.S. FLIP FLOP
REMOTE RESET
RESET SWITCH
REMOTE HOLD
STORAGE
STORAGE (REF. ONLY)
FOR REFERENCE ONLY
DISPLAY TIME
CONTROL LOGIC
MARKER
MODELS 80108, 80308
START/STOP LOGIC
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
REF. OUT
10 MHz
f/n (SCALED OUT)
M CLEAR
UPDATE
PRINT
ARM
GATE
START
STOP

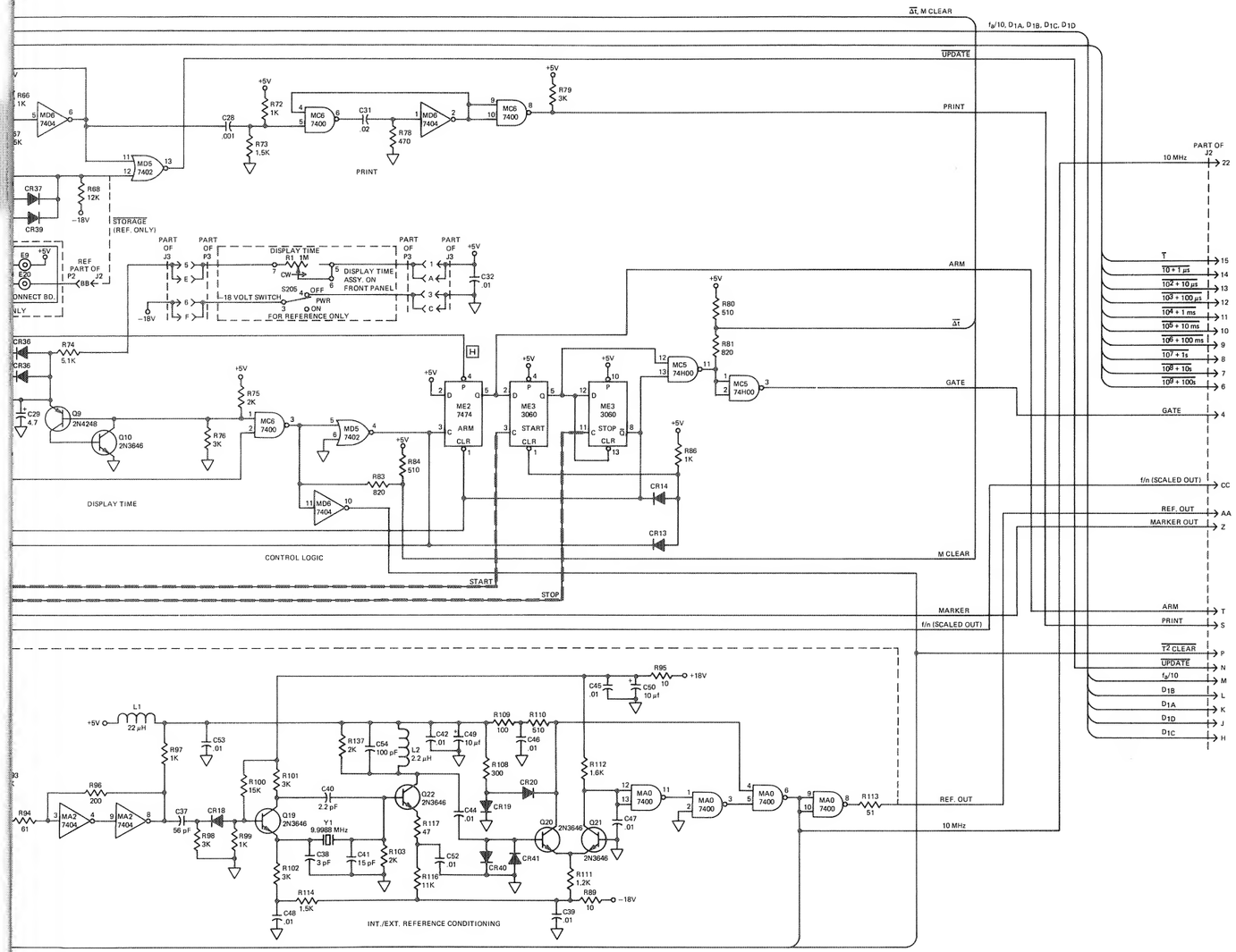

ΔT, M CLEAR
UPDATE
PRINT
ARM
GATE
MARKER
f/n (SCALED OUT)
START
STOP
CONTROL LOGIC
DISPLAY TIME
INT./EXT. REFERENCE CONDITIONING
PART OF J2
10 MHz
REF. OUT
T2 CLEAR
M CLEAR
f/n (SCALED OUT)
REF. OUT
MARKER OUT
ARM
PRINT
UPDATE
10 MHz
STORAGE (REF. ONLY)
DISPLAY TIME R1 1M
18 VOLT SWITCH
S205
OFF
PWR
ON
FOR REFERENCE ONLY
DISPLAY TIME ASSY. ON FRONT PANEL
REF PART OF P2
J2
P3
J3
MD6 7404
MD5 7402
MC6 7400
MC5 74H00
ME3 7474
ME3 3060
MA0 7400
MA2 7404
Q9 2N4248
Q10 2N3646
Q19 2N3646
Q20 2N3646
Q21 2N3646
Q22 2N3646
Y1 9.9988 MHz
L1 22 μH
L2 2.2 μH

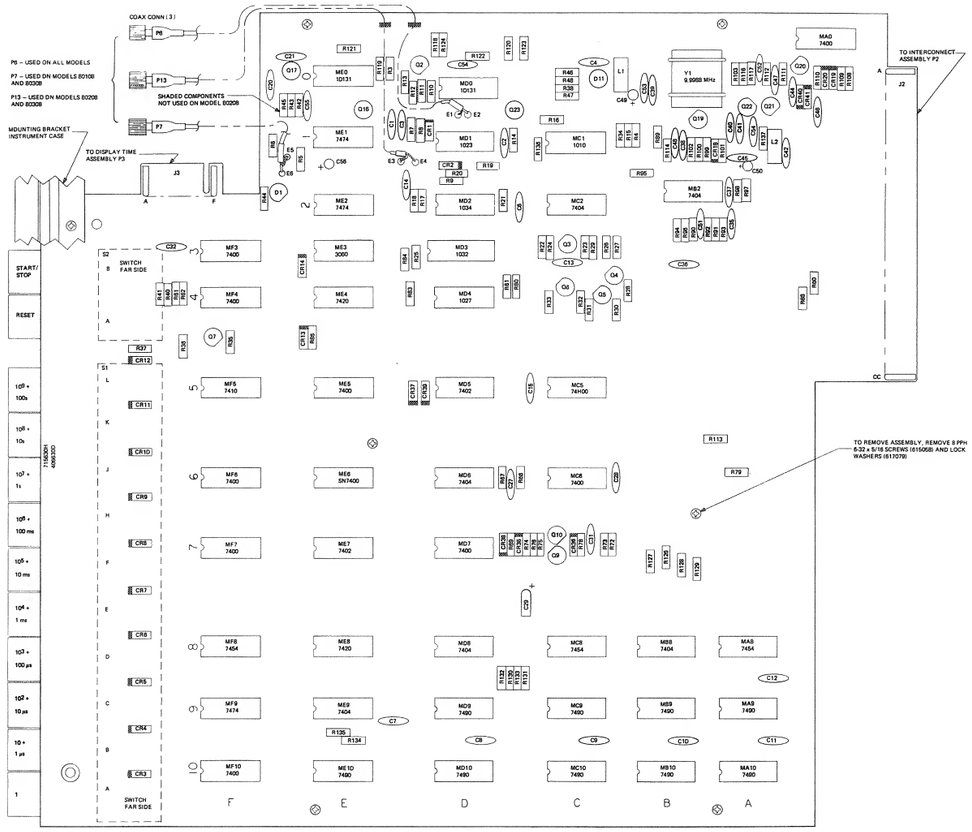

COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80308
P13 – USED ON MODELS 80208 AND 80308
SHADED COMPONENTS NOT USED ON MODEL 80208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6150S6) AND LOCK WASHERS (6170T9)
Y1 9.9988 MHz
START/ STOP
RESET
SWITCH FAR SIDE
MAD 7400

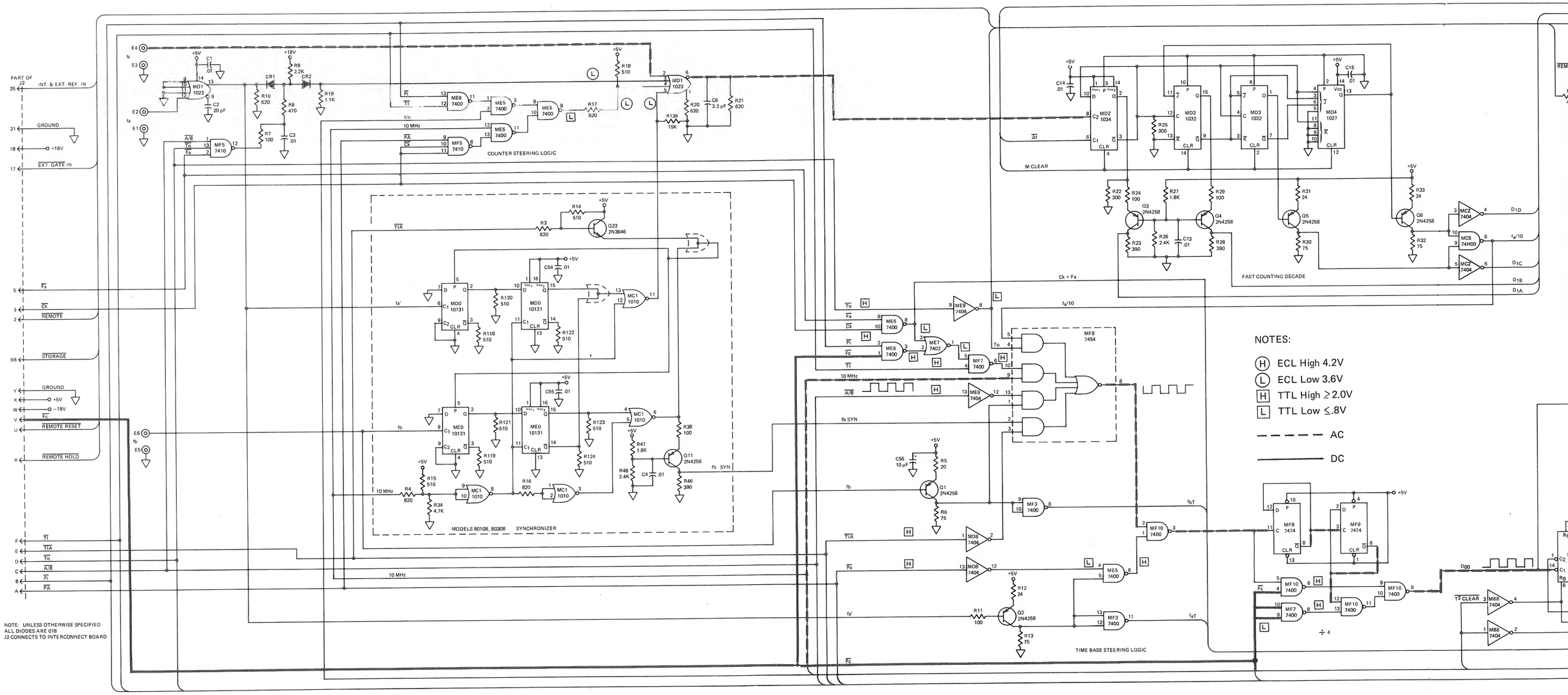

PART OF J2
INT. & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
REMOTE
STORAGE
GROUND
+5V
−18V
REMOTE RESET
REMOTE HOLD
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD
COUNTER STEERING LOGIC
MODELS 80108, 80308 SYNCHRONIZER
TIME BASE STEERING LOGIC
FAST COUNTING DECADE
M CLEAR
÷ 4
NOTES:
(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤ .8V
AC
DC


NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
REMOTE
M CLEAR
FAST COUNTING DECADE
MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
RECLOCKING LOGIC
TIME BASE STEERING LOGIC
MULTIPLIER/TIME BASE DECADES
÷ 4


EXT. GATE IN
START/STOP SWITCH
START/STOP
REMOTE RESET
RESET SWITCH
RESET R.S. FLIP FLOP
STORAGE
STORAGE (REF. ONLY)
REAR PANEL
INTERCONNECT BD.
FOR REFERENCE ONLY
DISPLAY TIME
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
PRINT
REMOTE HOLD
CONTROL LOGIC
MARKER
MODELS 8010B, 8030B
START/STOP LOGIC
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
M CLEAR
UPDATE
ARM
GATE
START
STOP
f/n (SCALED OUT)
REF. OUT
10 MHz


ΔT, M CLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
ΔT
GATE
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
T2 CLEAR
REF. OUT
10 MHz
PART OF J2
10 MHz
T
10⁰ + 1 µs
10² + 10 µs
10³ + 100 µs
10⁴ + 1 ms
10⁵ + 10 ms
10⁶ + 100 ms
10⁷ + 1s
10⁸ + 10s
10⁹ + 100s
f/n (SCALED OUT)
REF. OUT
MARKER OUT
ARM
PRINT
T2 CLEAR
UPDATE
f0/10
D1B
D1A
D1D
D1C
STORAGE (REF. ONLY)
DISPLAY TIME
18 VOLT SWITCH
DISPLAY TIME ASSY. ON FRONT PANEL
FOR REFERENCE ONLY
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 6010B AND 6020B
P13 – USED ON MODELS 6020B AND 6030B
SHADED COMPONENTS NOT USED ON MODEL 6020B
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (61506B) AND LOCK WASHERS (6152Y9)
START/ STOP
RESET
SWITCH FAR SIDE
SWITCH FAR SIDE


PART OF J2
INT. & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
GROUND
+5V
−18V
REMOTE RESET
REMOTE HOLD
STORAGE
REMOTE
COUNTER STEERING LOGIC
MODELS 8010B, 8030B SYNCHRONIZER
M CLEAR
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
10 MHz
fb SYN
Ck + Fa
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤.8V
AC
DC
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

NOTES:

(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤.8V
AC
DC

FAST COUNTING DECADE

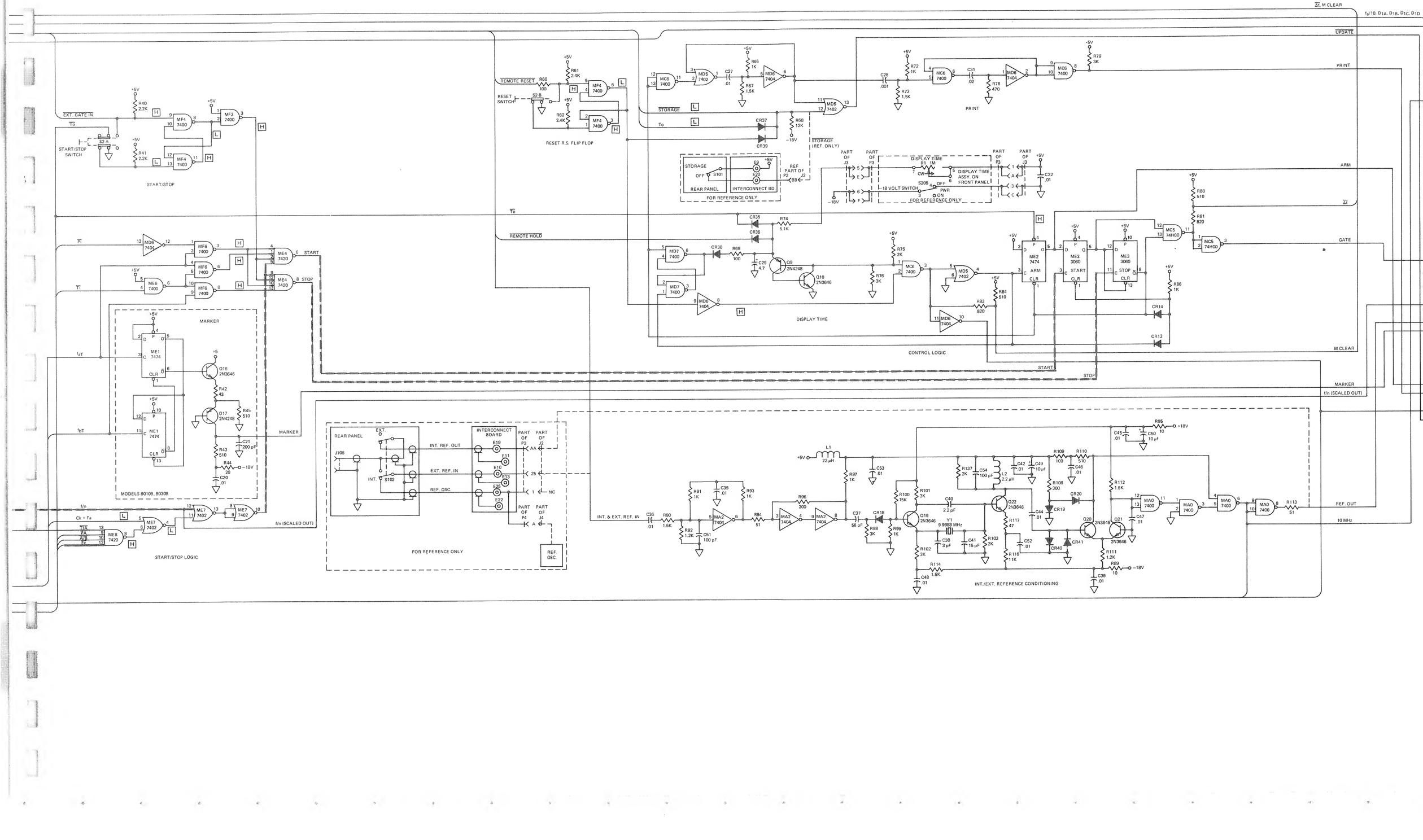
TIME BASE STEERING LOGIC

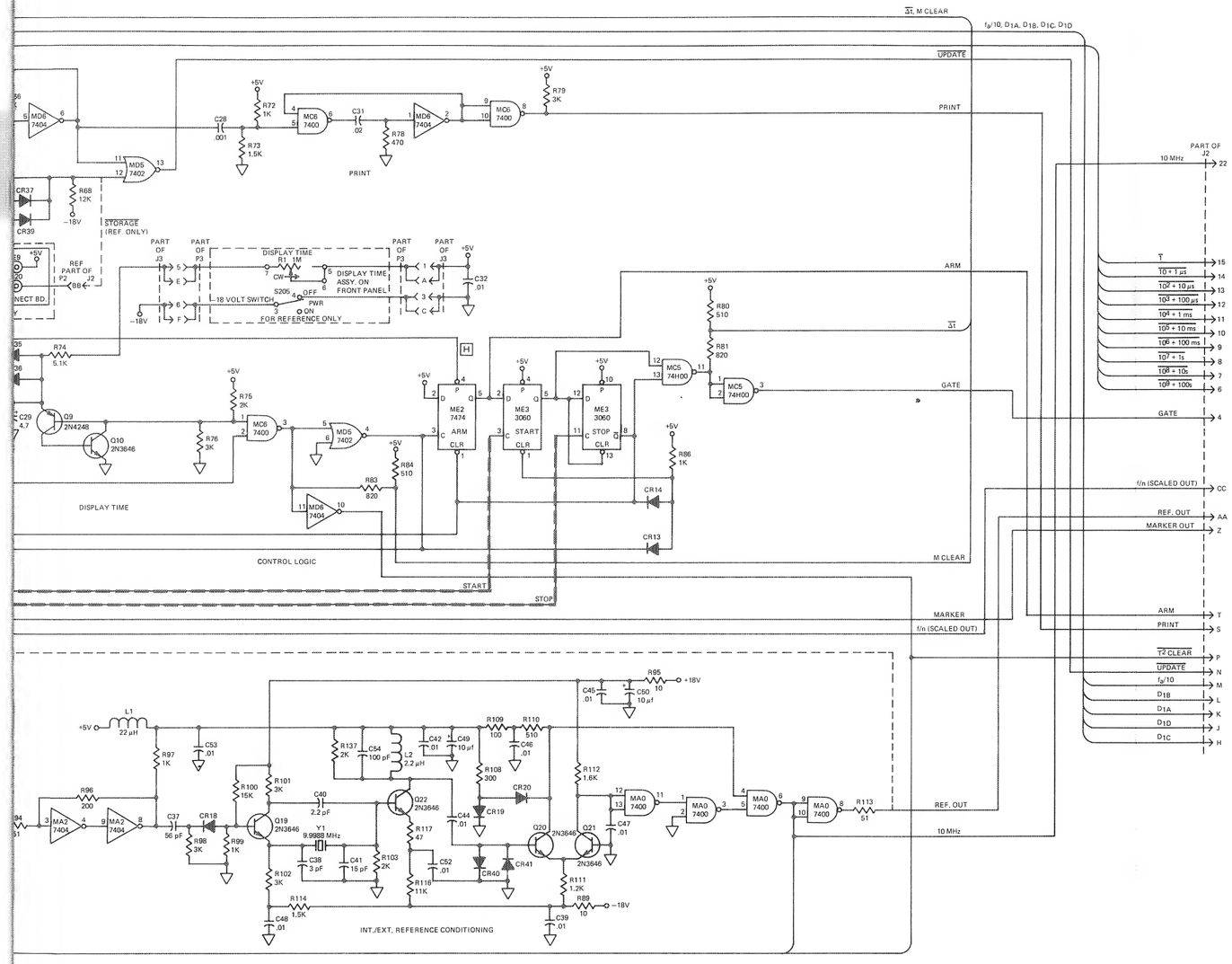
MULTIPLIER/TIME BASE SWITCHING

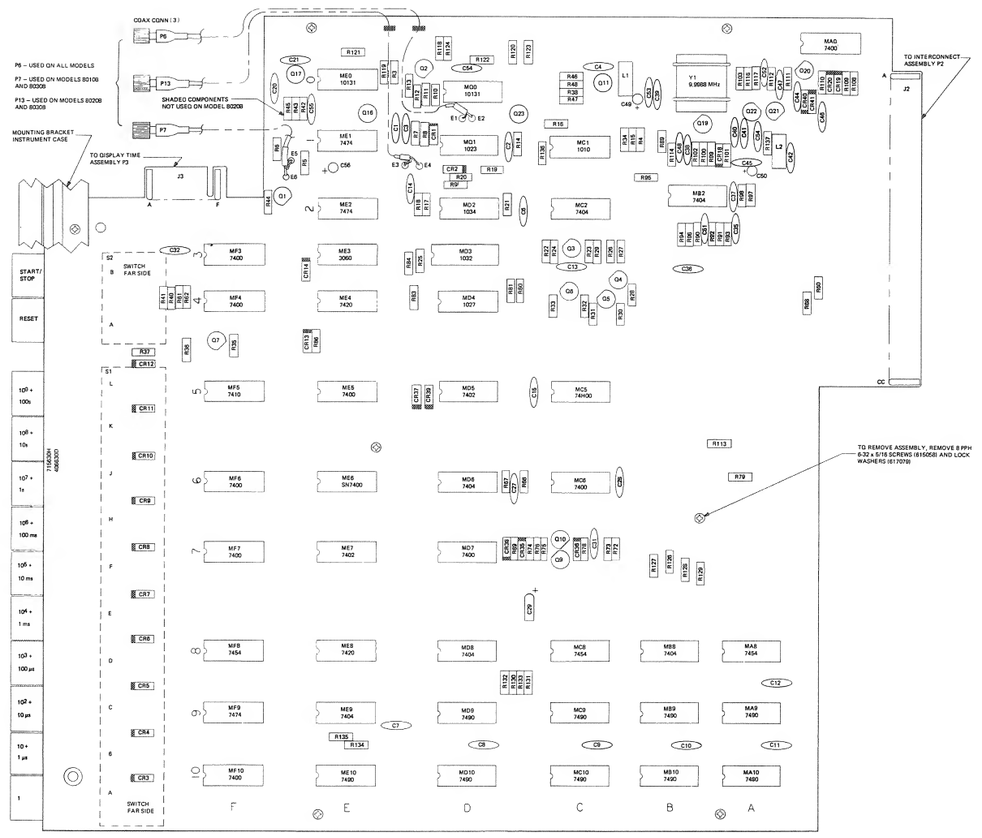
MULTIPLIER/TIME BASE GATING

RECLOCKING LOGIC

MULTIPLIER/TIME BASE DECADES


EXT. GATE IN
START/STOP SWITCH
START/STOP
REMOTE RESET
RESET SWITCH
RESET R.S. FLIP FLOP
STORAGE
STORAGE (REF. ONLY)
REAR PANEL
INTERCONNECT BD.
FOR REFERENCE ONLY
18 VOLT SWITCH
DISPLAY TIME
DISPLAY TIME ASSY. ON FRONT PANEL
PRINT
REMOTE HOLD
CONTROL LOGIC
MARKER
MODELS 80108, 80308
START/STOP LOGIC
INT. REF. OUT
EXT. REF. IN
REF. OSC.
FOR REFERENCE ONLY
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
M CLEAR
UPDATE
ARM
GATE
START
STOP
REF. OUT
10 MHz


Δt, M CLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
Δt
GATE
f/n (SCALED OUT)
REF. OUT
MARKER OUT
M CLEAR
START
STOP
MARKER
T2 CLEAR
10 MHz
PART OF J2
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
18 VOLT SWITCH
DISPLAY TIME ASSY. ON FRONT PANEL
FOR REFERENCE ONLY
MD5 7404
MC6 7400
MD6 7404
MC5 7400
MD5 7402
MD6 7402
MC5 74H00
MA0 7400
MA2 7404
ME2 7474 ARM
ME3 3060 START
ME3 3060 STOP
Q9 2N4248
Q10 2N3646
Q19 2N3646
Q20 2N3646
Q21 2N3646
Q22 2N3646
Y1 9.9988 MHz
L1 22 µH
L2 2.2 µH
+5V
−18V
+18V


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 8010B AND 8030B
P13 – USED ON MODELS 8020B AND 8030B
SHADED COMPONENTS NOT USED ON MODEL 8020B
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (8160582) AND LOCK WASHERS (8170709)
9.9988 MHz
START/ STOP
RESET
SWITCH FAR SIDE
71150304 4966300

PART OF J2

INT. & EXT. REF. IN — 25

GROUND — 21

+18V — 19

EXT. GATE IN — 17

$\overline{Fa}$ — 5

$\overline{Ck}$ — 3

REMOTE — 2

STORAGE — BB

GROUND — Y

+5V — X

−18V — W

$\overline{Fc}$ — V

REMOTE RESET — U

REMOTE HOLD — R

$\overline{Ti}$ — F

$\overline{TiA}$ — E

$\overline{To}$ — D

$\overline{A/B}$ — C

$\overline{Pi}$ — B

$\overline{PA}$ — A

NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

E4 fc
E3
E2
fa
E1

MD1 1023 — C1 .01 — C2 20 pF

+18V — R9 2.2K — CR1 — CR2 — R19 1.1K — R10 620 — R8 470 — R7 100 — C3 .01

MF5 7410 — $\overline{A/B}$ — $\overline{To}$ — $\overline{Fa}$

ME6 7400 — $\overline{Pi}$ — $\overline{Ti}$

ME5 7400 — f/n — 10 MHz

ME5 7400 — $\overline{PA}$ — $\overline{Ck}$

MF5 7410

COUNTER STEERING LOGIC

+5V — R18 510 — MD1 1023 — R20 620 — C6 3.3 pF — R21 620 — R136 15K — R17 820

MODELS 80108, 8030B SYNCHRONIZER

$\overline{TiA}$ — R3 820 — R14 510 — Q23 2N3646

fa' — MD0 10131 — C54 .01 — R120 510 — R118 510 — MC1 1010 — R122 510

MD0 10131 — C55 .01 — R121 510 — R119 510 — R123 510 — R124 510

fb — E6
E5

MC1 1010 — R38 100 — R47 1.8K — R48 2.4K — C4 .01 — Q11 2N4258 — R46 390 — fb SYN

10 MHz — R4 820 — R34 4.7K — R15 510 — R16 820

$\overline{Fa}$ — $\overline{Ck}$ — ME6 7400 — ME8 7404 — $\overline{To}$ — f$_a$/10

$\overline{Pi}$ — $\overline{Fc}$ — ME6 7400 — ME7 7402 — MF7 7400 — $\overline{Ti}$

10 MHz — $\overline{A/B}$ — ME9 7404 — fb SYN

C56 10 µF — R5 20 — Q1 2N4258 — R6 75 — fb

MD8 7404 — $\overline{TiA}$

MD8 7404 — $\overline{Pa}$

fa' — R11 100 — Q2 2N4258 — R12 24 — R13 75

$\overline{Fc}$

MF8 7454

MF3 7400 — f$_b$T

MF10 7400 — MF3 7400 — f$_a$T

TIME BASE STEERING LOGIC

+5V — C14 .01 — MD2 1034 — C15 .01 — MD3 1032 — MD3 1032 — MD4 1027

$\overline{\Delta t}$ — M CLEAR

R22 300 — R24 100 — R27 1.8K — R29 100 — R31 24 — R33 24

Q3 2N4258 — Q4 2N4258 — Q5 2N4258 — Q6 2N4258

R23 390 — R26 2.4K — C13 .01 — R28 390 — R30 75 — R32 75

FAST COUNTING DECADE

Ck + Fa

MC2 7404 — D_{1D} — MC5 74H00 — f$_a$/10 — MC2 7404 — D_{1C} — D_{1B} — D_{1A}

REMOTE — R35 4.7K

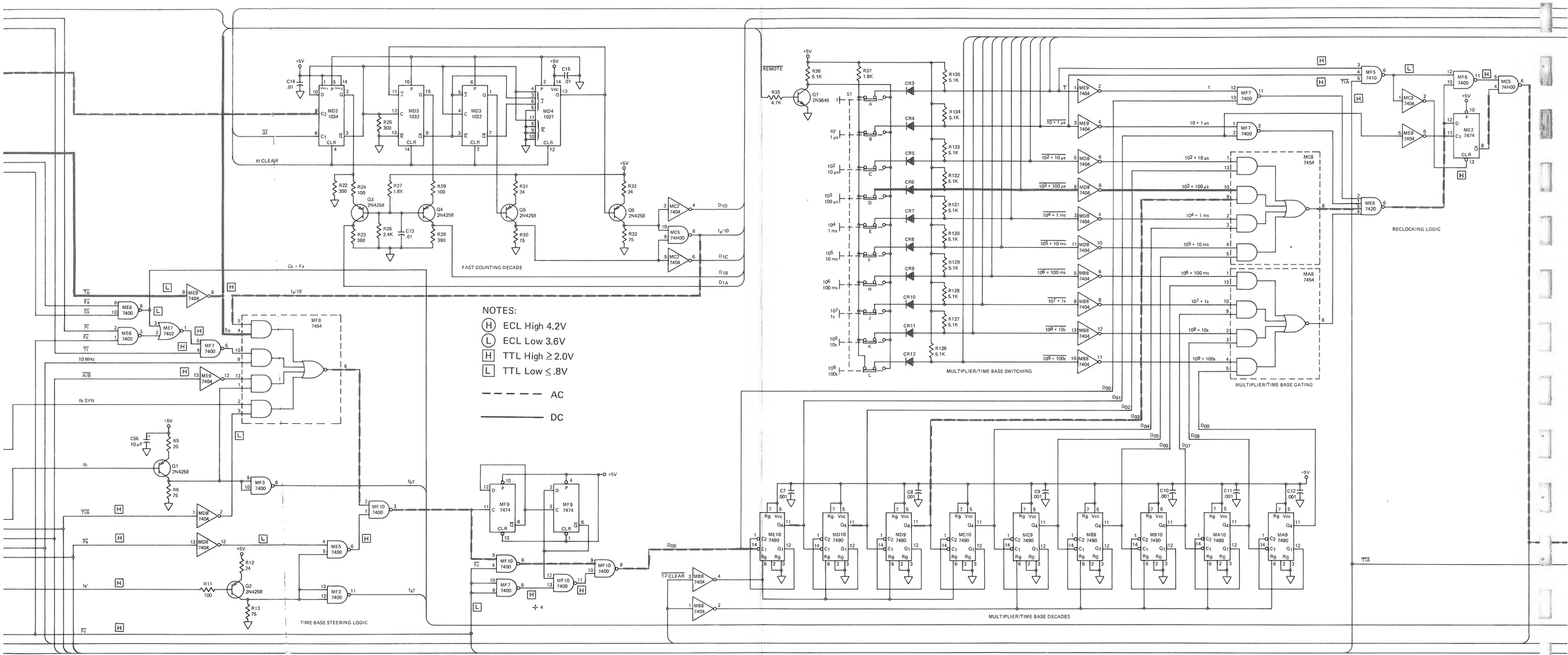
MF9 7474 — MF9 7474 — MF10 7400 — MF10 7400 — MF10 7400 — MF7 7400 — MF10 7400 — ÷ 4

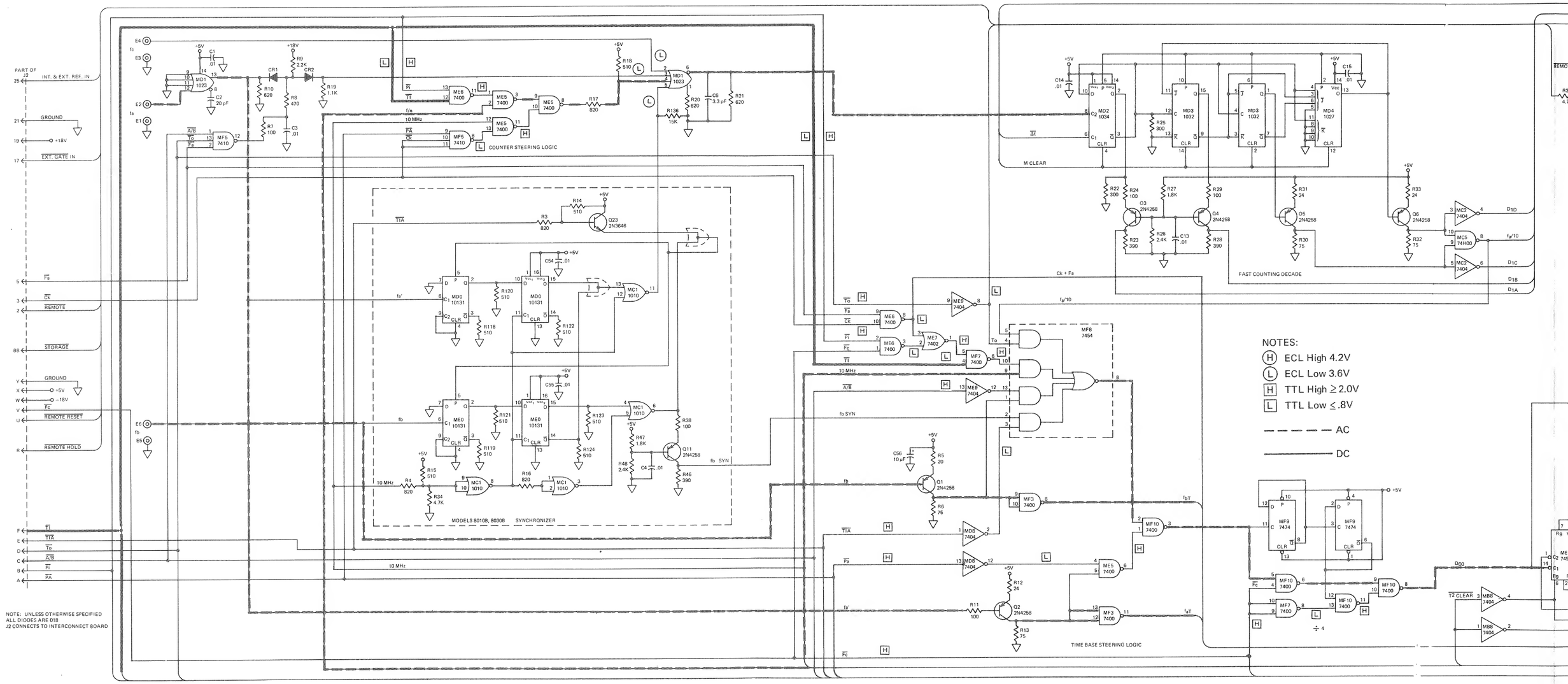
D_{00} — $\overline{T2}$ CLEAR — M88 7404 — M88 7404

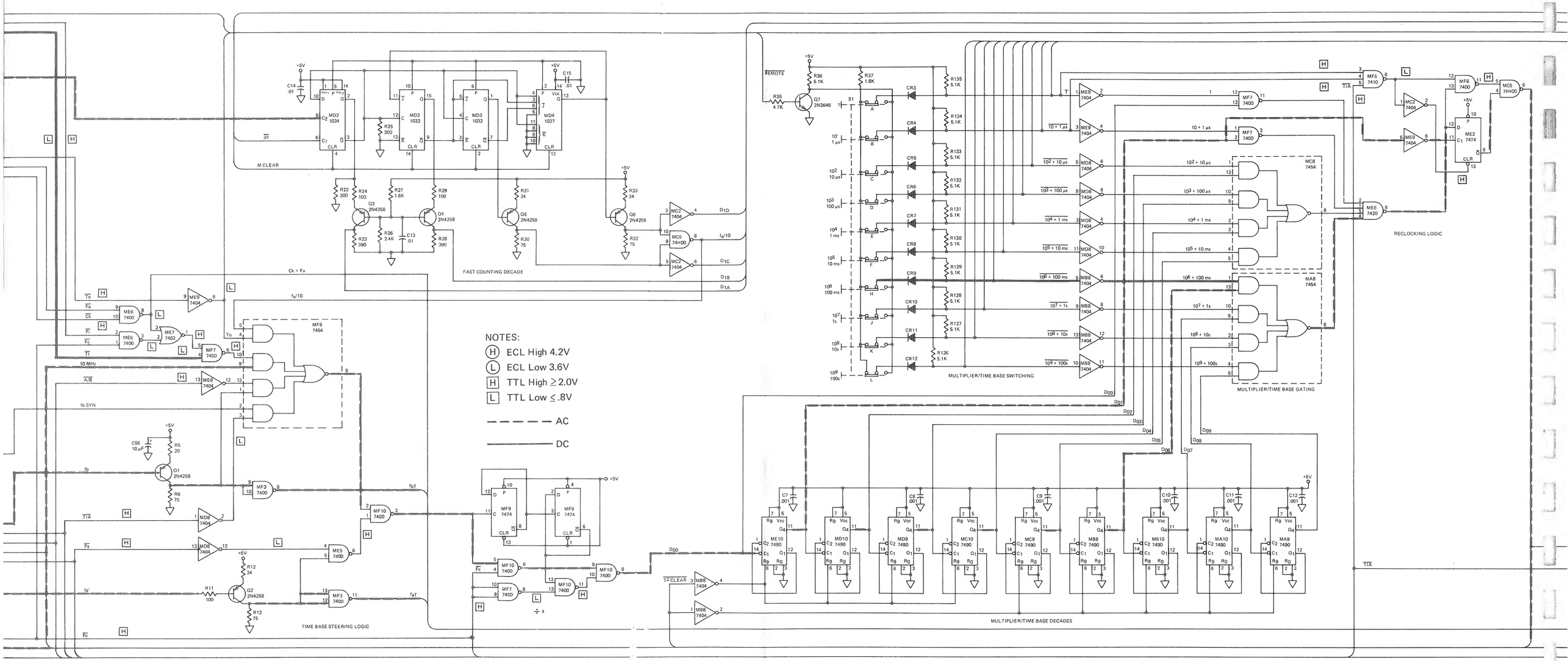
ME10 7490 — C7 .001 — Rg Vcc Q4 Q1 Rg Rg Q2

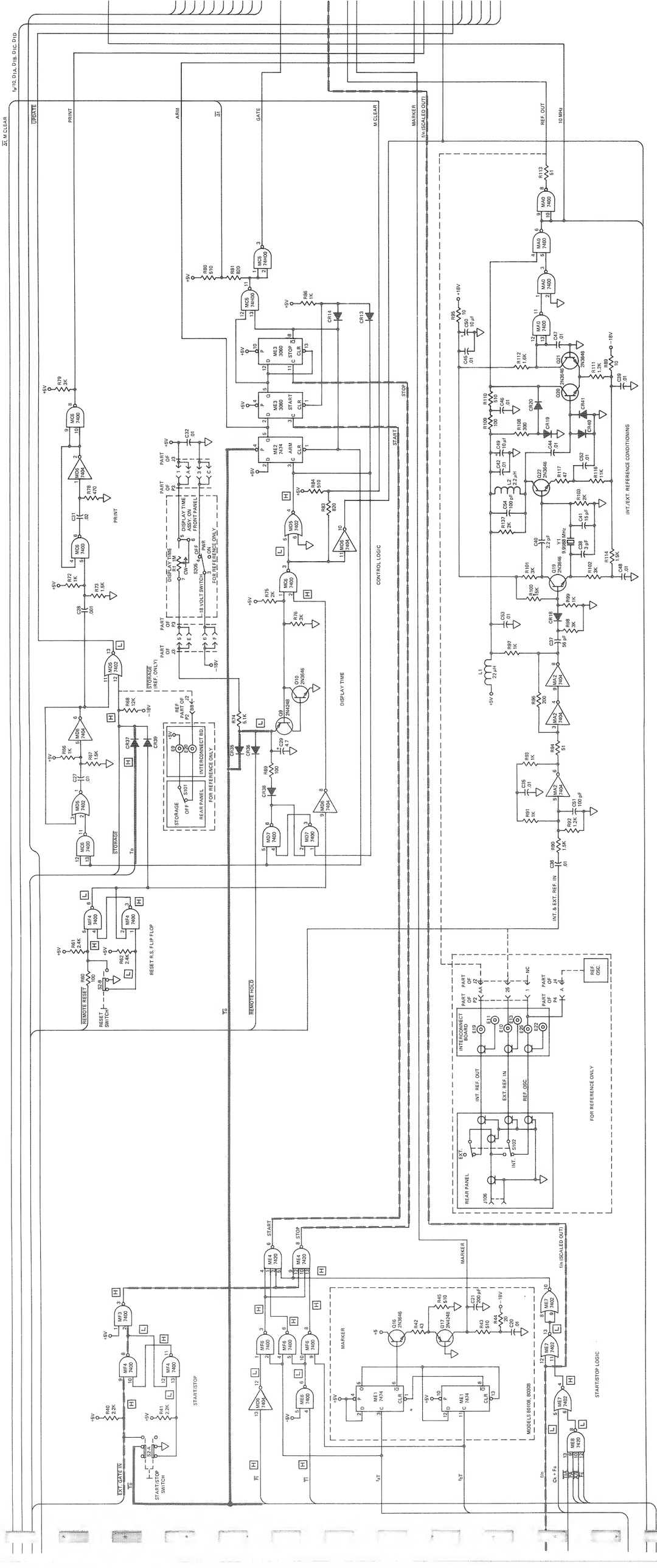
NOTES:

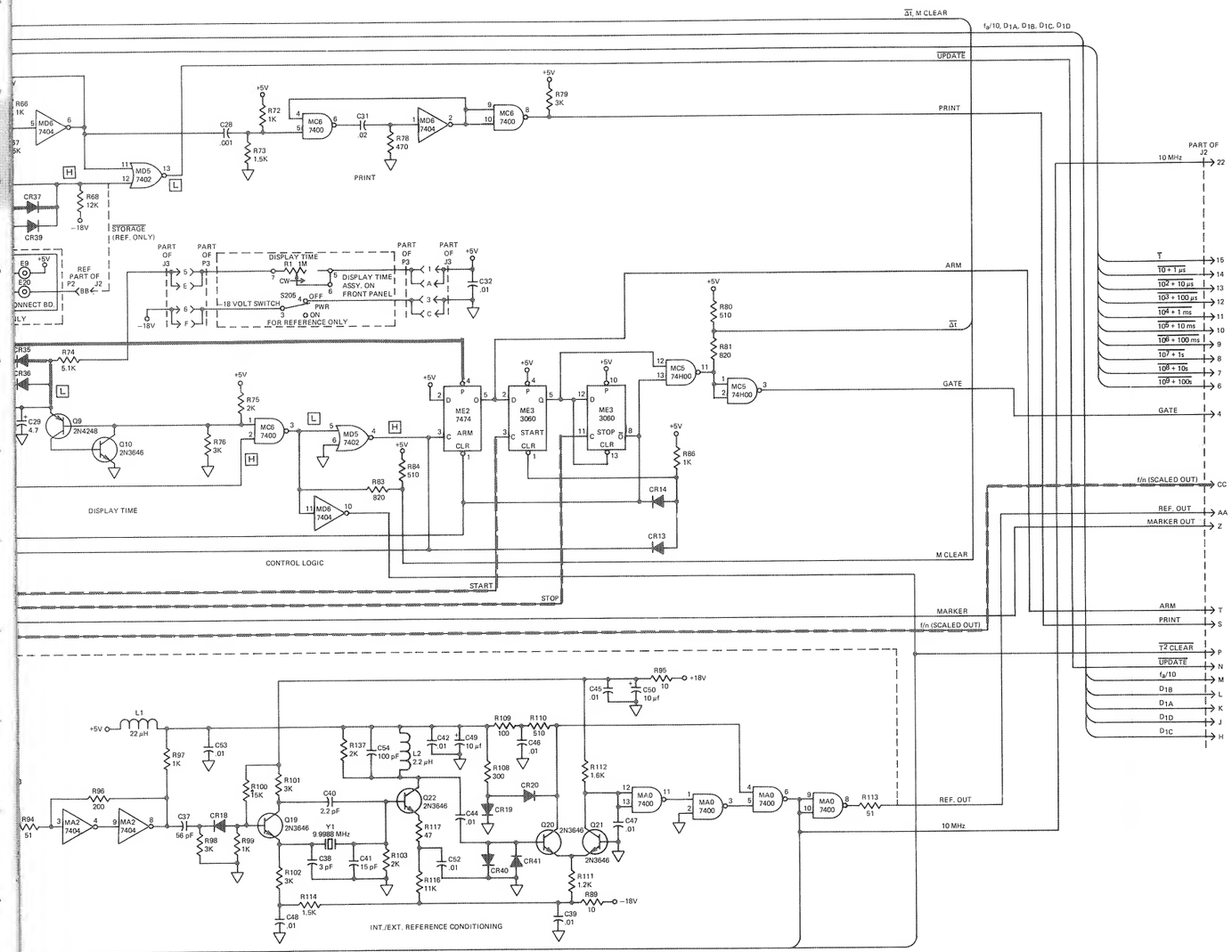
(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤ .8V
– – – – AC
——— DC

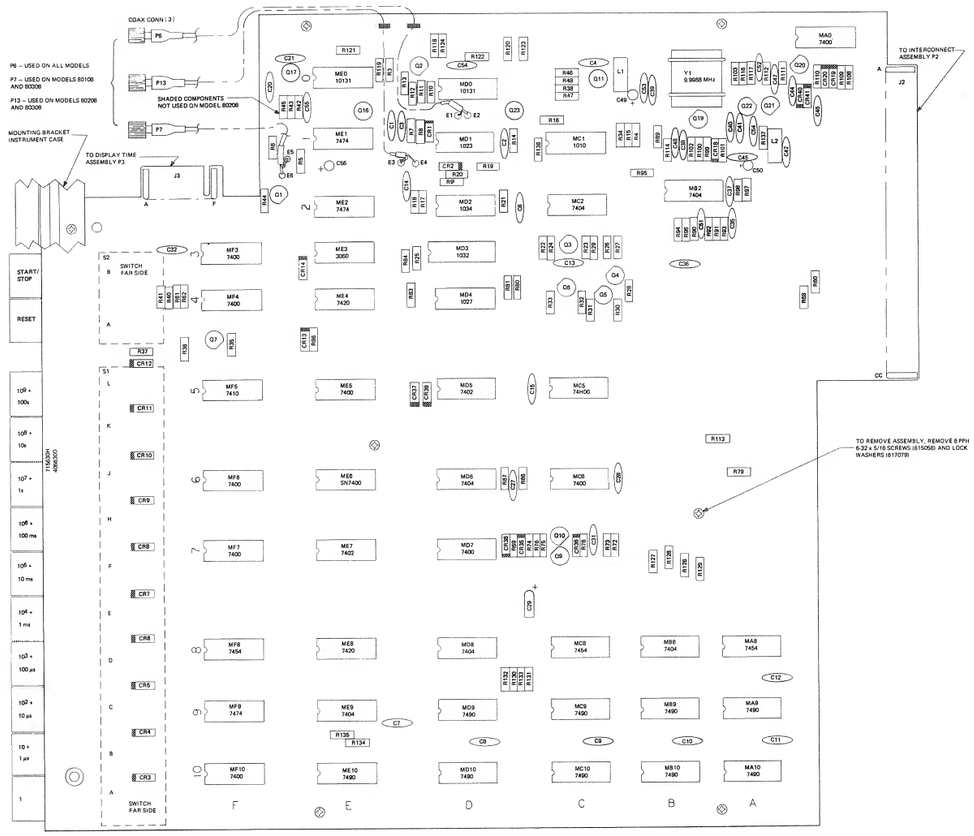

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
FAST COUNTING DECADE
MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
RECLOCKING LOGIC
TIME BASE STEERING LOGIC
MULTIPLIER/TIME BASE DECADES
REMOTE
M CLEAR
Ck ÷ Fa
fb SYN
10 MHz
÷ 4

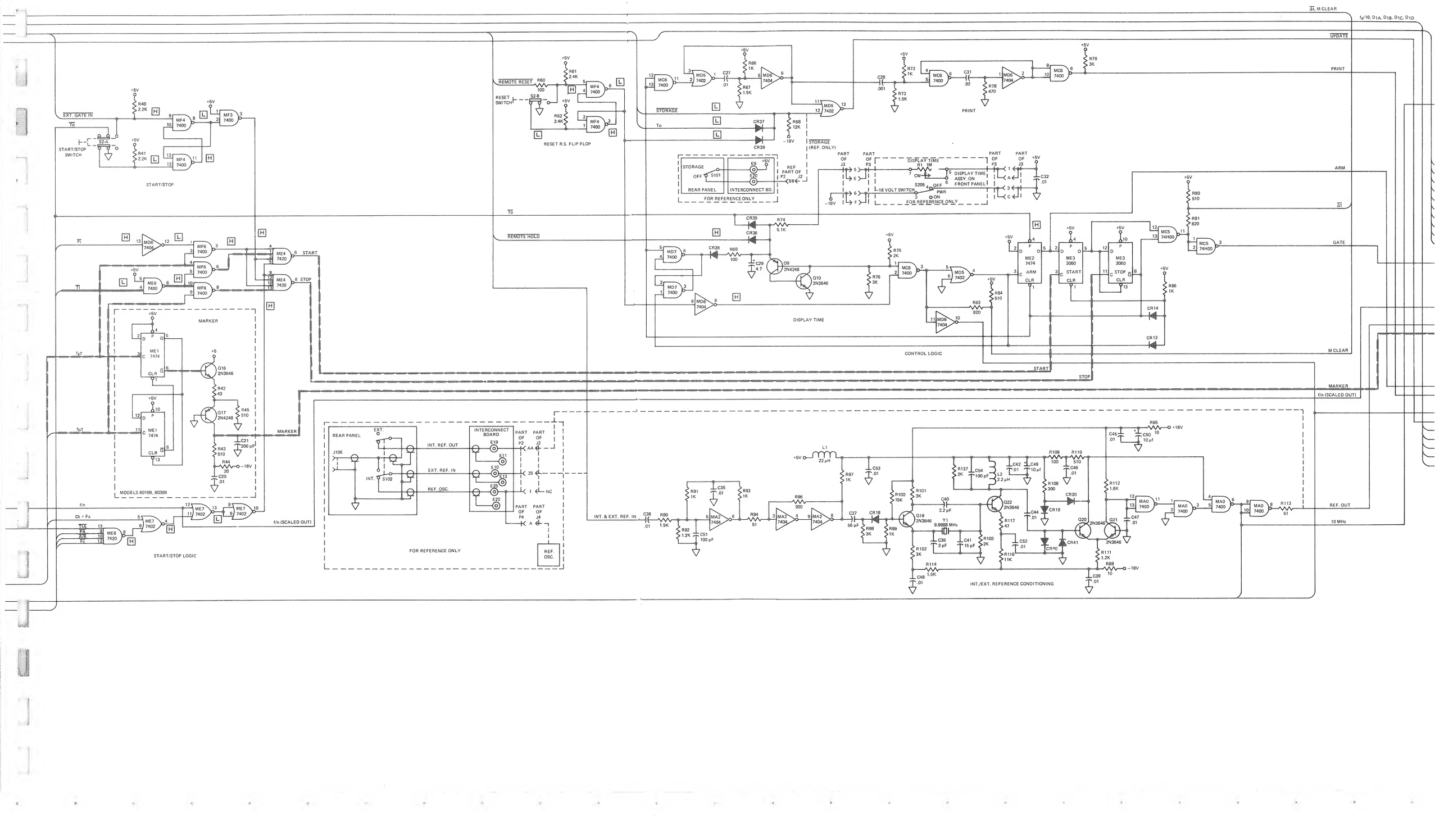

PART OF J2
INT. & EXT. REF. IN
GROUND
+18V
EXT. GATE IN
Fa
fa
REMOTE
STORAGE
GROUND
+5V
−18V
Fc
REMOTE RESET
REMOTE HOLD
TI
TIA
To
A/B
Pi
PA
10 MHz
fc
fa
fb
E1
E2
E3
E4
E5
E6
MD1 1023
MF5 7410
ME6 7400
ME5 7400
COUNTER STEERING LOGIC
MODELS 8010B, 80308 SYNCHRONIZER
MD0 10131
MC1 1010
Q23 2N3646
Q11 2N4258
MF8 7454
MF7 7400
MF3 7400
MD8 7404
ME8 7404
ME7 7402
Q1 2N4258
Q2 2N4258
TIME BASE STEERING LOGIC
MD2 1034
MD3 1032
MD4 1027
M CLEAR
Q3 2N4258
Q4 2N4258
Q5 2N4258
Q6 2N4258
FAST COUNTING DECADE
MC2 7404
MC5 74H00
MF9 7474
MF10 7400
MB8 7404
ME10 7490
÷ 4
T2 CLEAR
REMOTE
NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

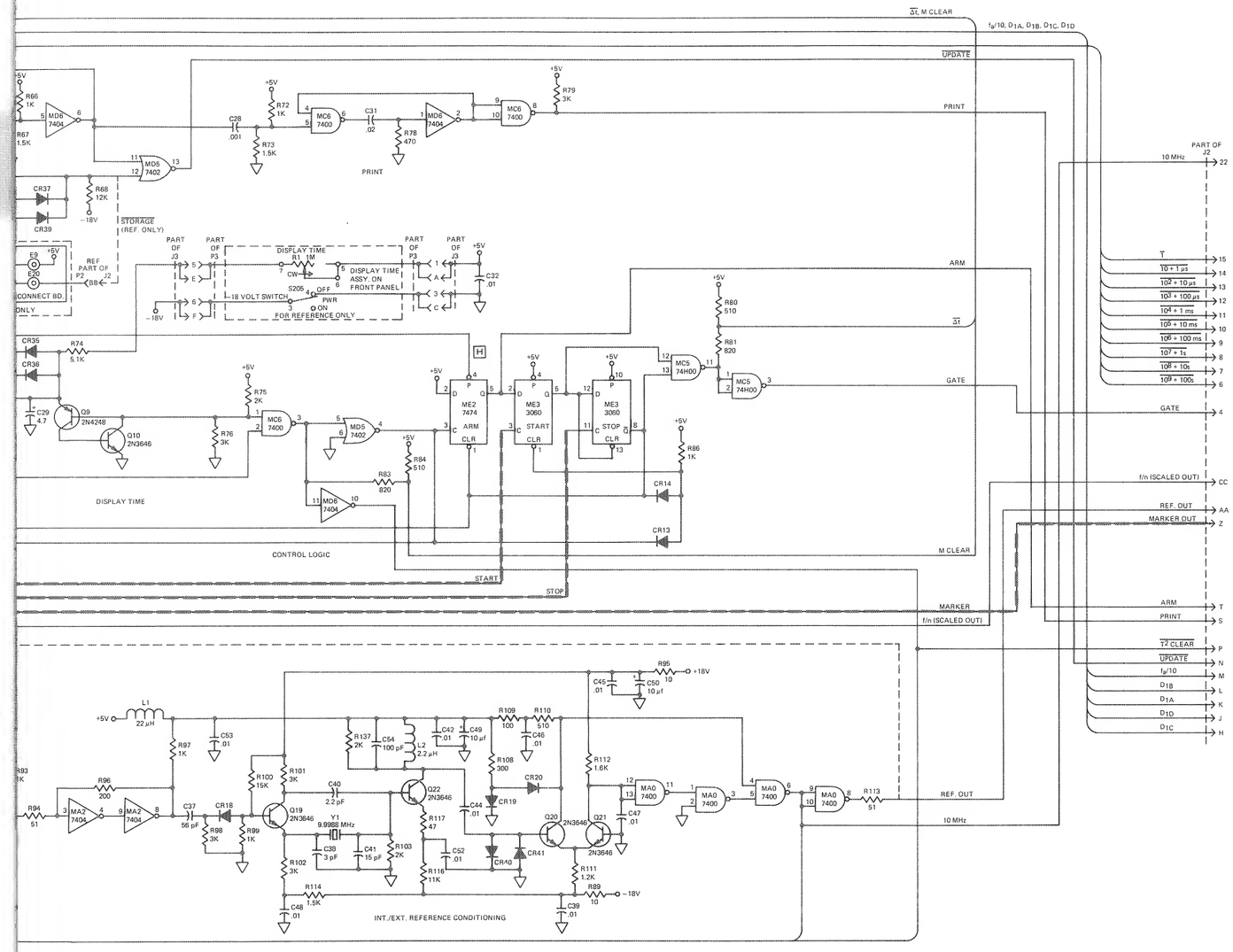

NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
MULTIPLIER/TIME BASE DECADES
RECLOCKING LOGIC
REMOTE
M CLEAR
10 MHz
fb SYN
÷ 4

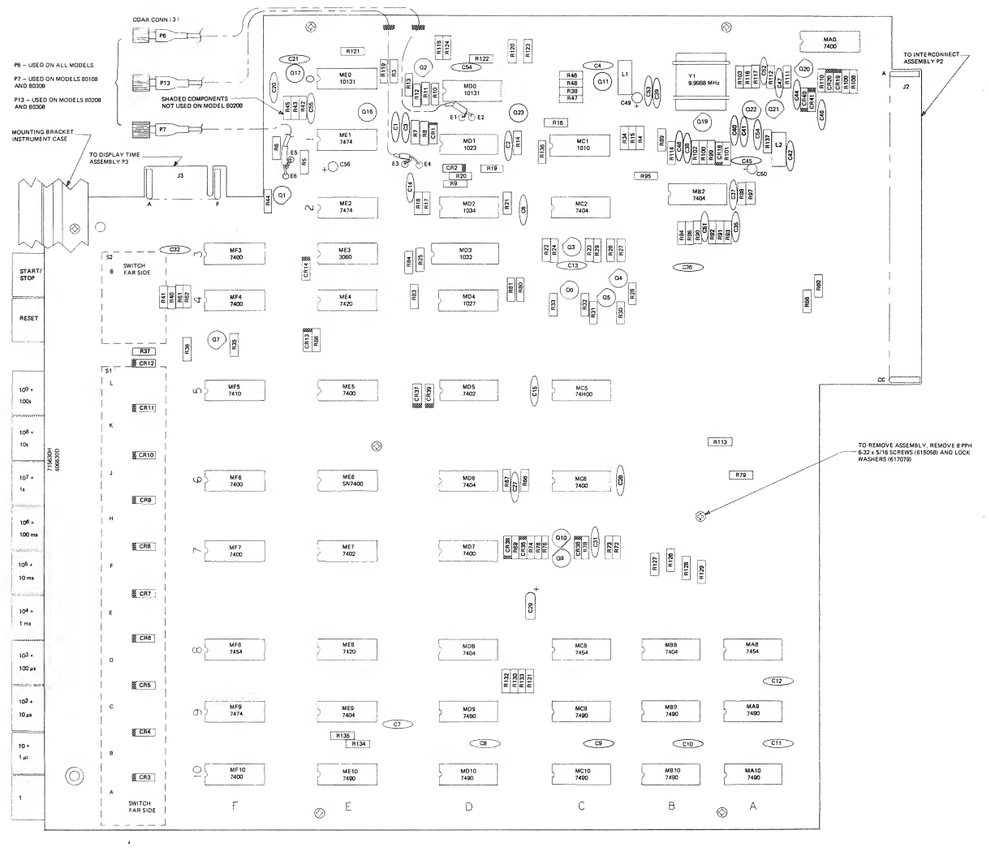

ΔT, M CLEAR
fo/10 D1A, D1B, D1C, D1D
UNGATE
PRINT
ARM
ΔT
GATE
M CLEAR
MARKER
f/n (SCALED OUT)
REF. OUT
10 MHz
CONTROL LOGIC
DISPLAY TIME
START
STOP
STORAGE (REF. ONLY)
18 VOLT SWITCH
FOR REFERENCE ONLY
INT./EXT. REFERENCE CONDITIONING
INT. & EXT. REF. IN
RESET R.S. FLIP FLOP
REMOTE RESET
RESET SWITCH
REMOTE HOLD
START/STOP
START/STOP SWITCH
EXT. GATE IN
MARKER
START/STOP LOGIC
MODELS 80108, 80208
INTERCONNECT BD.
REAR PANEL
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INTERCONNECT BOARD
REF OSC


ΔT, M CLEAR
fM/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
ΔT
GATE
GATE
f/n (SCALED OUT)
REF. OUT
MARKER OUT
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
ARM
PRINT
T2 CLEAR
UPDATE
fM/10
D1B
D1A
D1D
D1C
REF. OUT
10 MHz
PART OF J2
10 MHz
T
10 + 1 µs
10² + 10 µs
10³ + 100 µs
10⁴ + 1 ms
10⁵ + 10 ms
10⁶ + 100 ms
10⁷ + 1s
10⁸ + 10s
10⁹ + 100s
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
PWR
FOR REFERENCE ONLY
REF PART OF P2 J2
CONNECT BD
ONLY
+5V
−18V
+18V


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80308
P13 – USED ON MODELS 80208 AND 80308
SHADED COMPONENTS NOT USED ON MODEL 80208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6150565) AND LOCK WASHERS (6120791)
START/ STOP
RESET
SWITCH FAR SIDE
SWITCH FAR SIDE
Y1 9.9888 MHz
F
E
D
C
B
A


EXT. GATE IN
START/STOP SWITCH
START/STOP
REMOTE RESET
RESET SWITCH
RESET R.S. FLIP FLOP
STORAGE
REAR PANEL
INTERCONNECT BD.
FOR REFERENCE ONLY
STORAGE (REF. ONLY)
DISPLAY TIME
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
REMOTE HOLD
DISPLAY TIME
CONTROL LOGIC
MARKER
MODELS 80108, 80308
START/STOP LOGIC
INTERCONNECT BOARD
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
UPDATE
PRINT
ARM
GATE
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
REF. OUT
10 MHz


Δt, M CLEAR
f9/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
Δt
GATE
DISPLAY TIME
CONTROL LOGIC
START
STOP
MARKER
f/n (SCALED OUT)
M CLEAR
PART OF J2
10 MHz
T
10 + 1 µs
10² + 10 µs
10³ + 100 µs
10⁴ + 1 ms
10⁵ + 10 ms
10⁶ + 100 ms
10⁷ + 1s
10⁸ + 10s
10⁹ + 100s
f/n (SCALED OUT)
REF. OUT
MARKER OUT
ARM
PRINT
T2 CLEAR
UPDATE
f9/10
D1B
D1A
D1D
D1C
REF. OUT
10 MHz
INT./EXT. REFERENCE CONDITIONING
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
FOR REFERENCE ONLY
CONNECT BD. ONLY
STORAGE (REF. ONLY)


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80308
P13 – USED ON MODELS 80208 AND 80308
SHADED COMPONENTS NOT USED ON MODEL 80208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6115058) AND LOCK WASHERS (6170791)
START/ STOP
RESET
SWITCH FAR SIDE
SWITCH FAR SIDE

NOTES:
(H) ECL High 4.2V
(L) ECL Low 3.6V
[H] TTL High ≥ 2.0V
[L] TTL Low ≤ .8V
– – – – – AC
——— DC

FAST COUNTING DECADE

COUNTER STEERING LOGIC

TIME BASE STEERING LOGIC

SYNCHRONIZER

MODELS 8010B, 8030B

÷ 4

M CLEAR

T2 CLEAR

REMOTE

REMOTE RESET

REMOTE HOLD

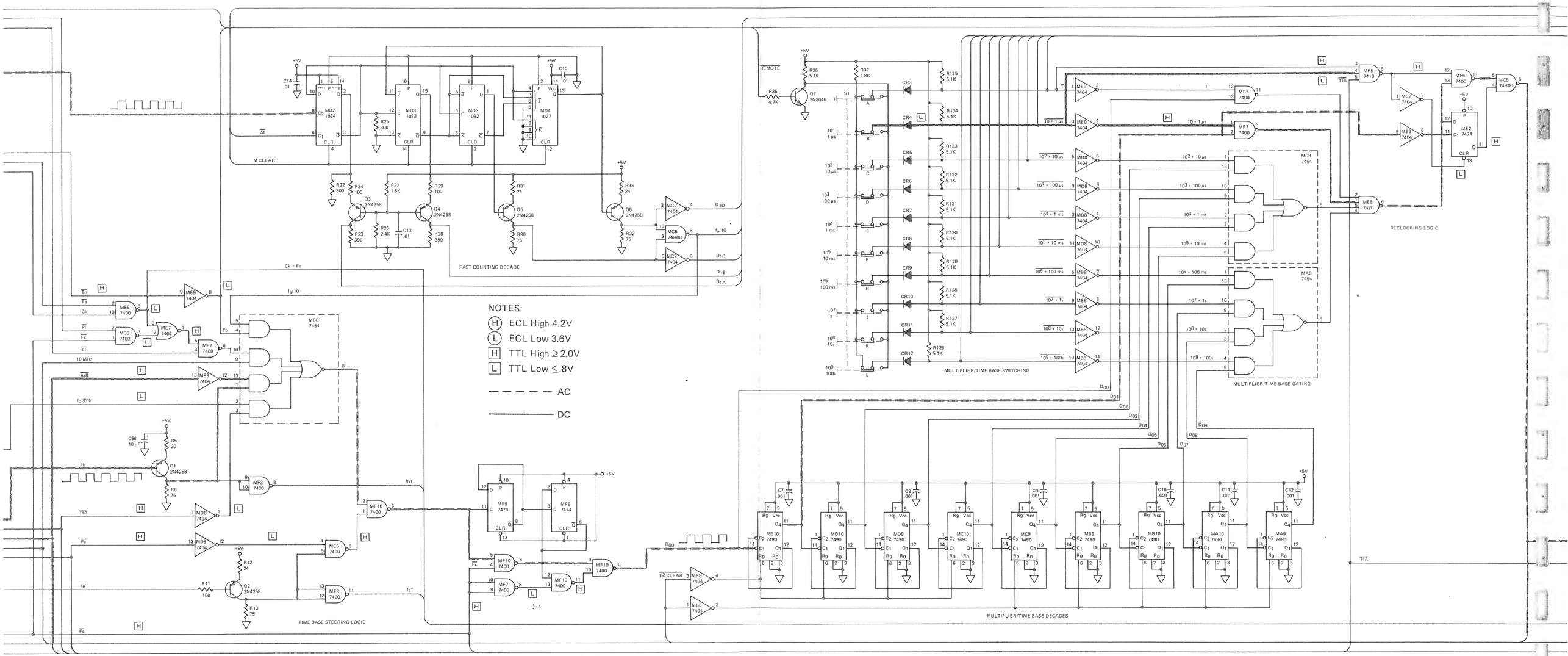
STORAGE

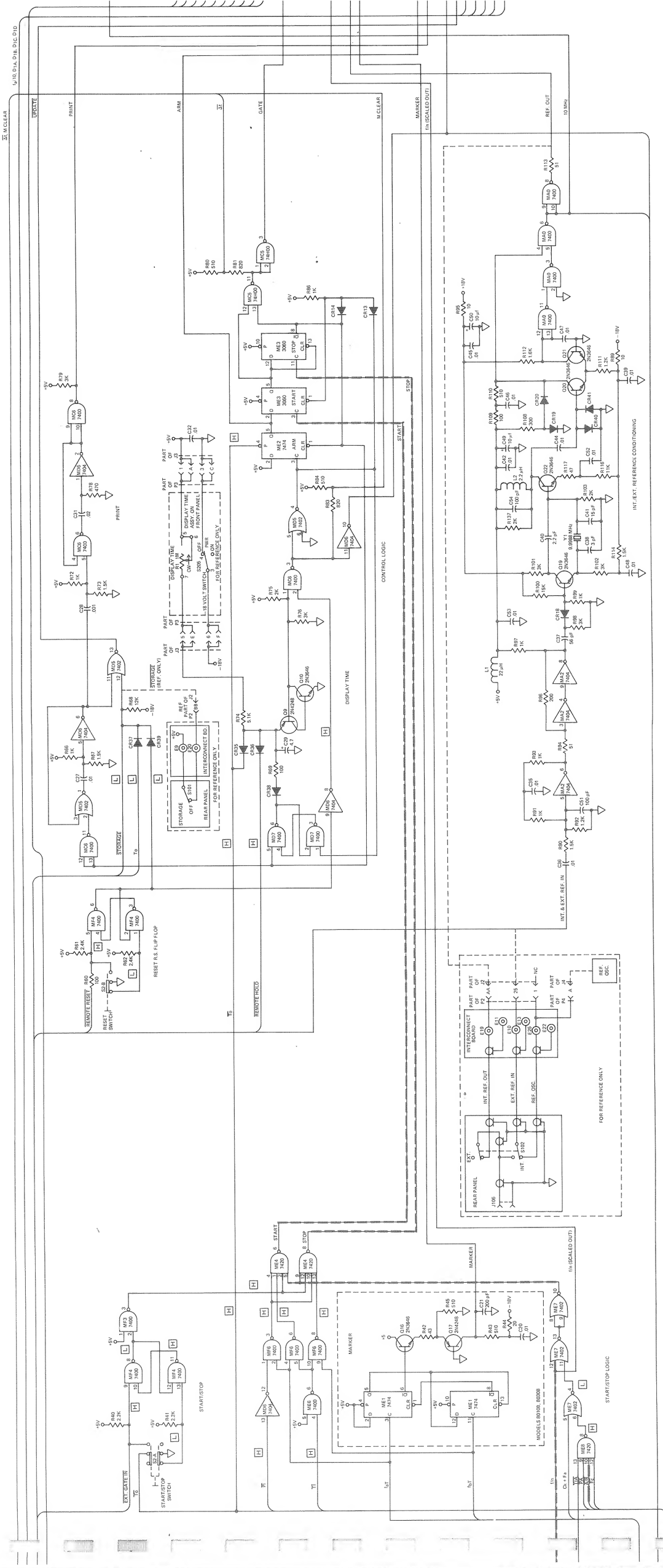
GROUND

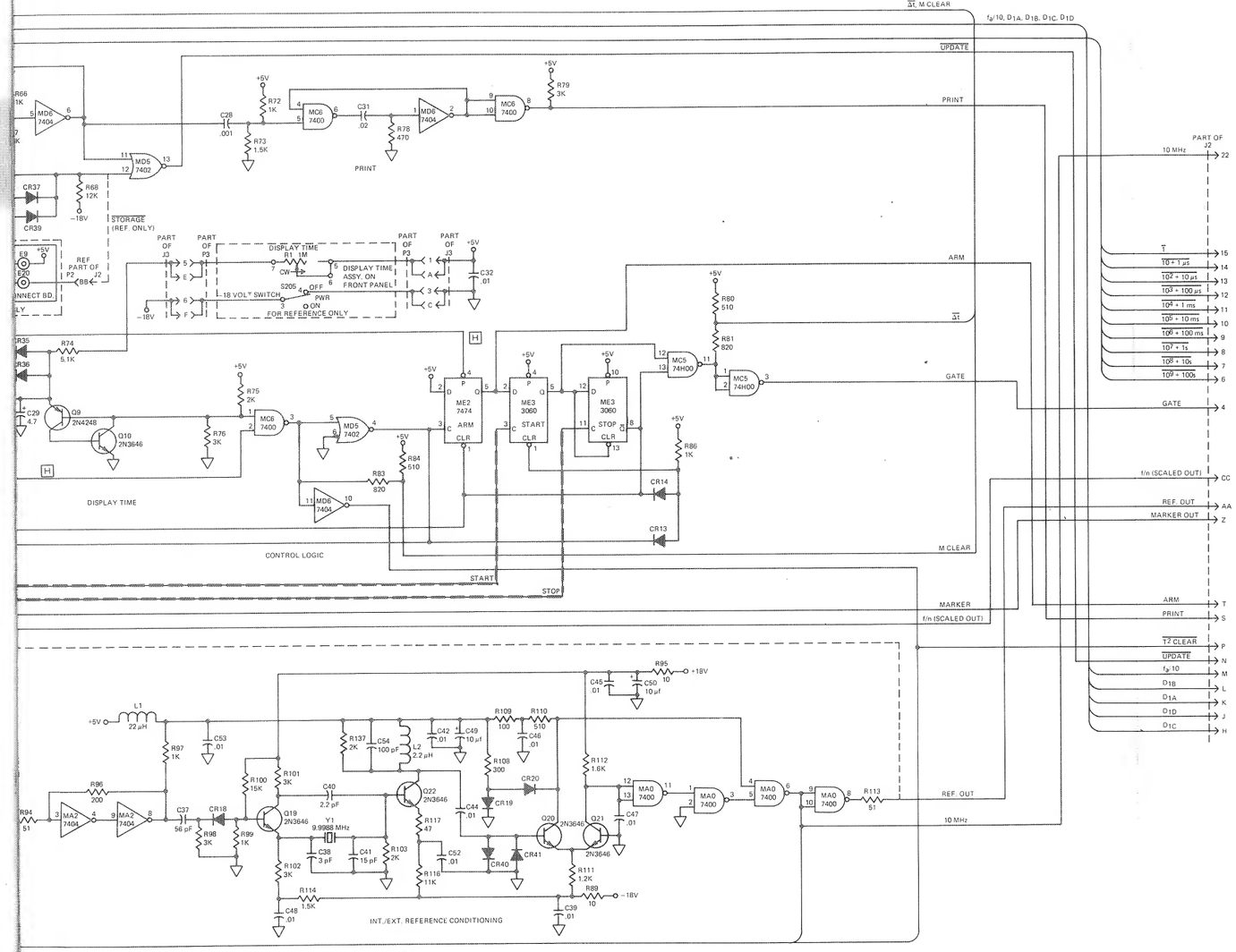
EXT. GATE IN

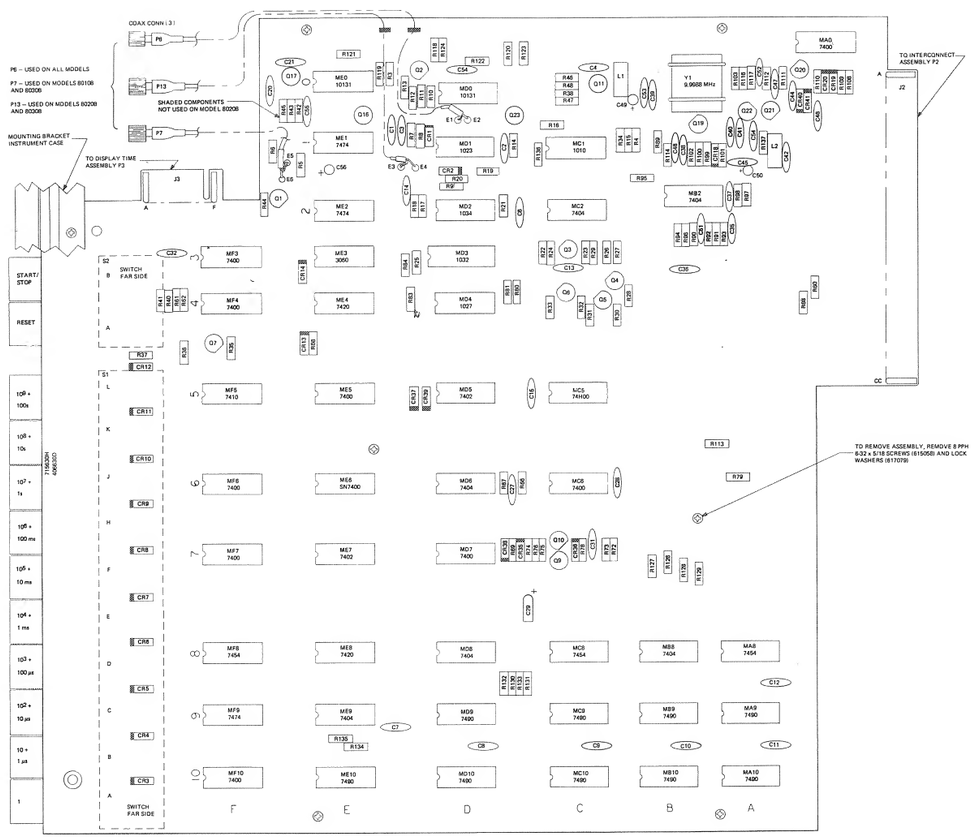
10 MHz

NOTE: UNLESS OTHERWISE SPECIFIED
ALL CODES ARE 8030B
J2 CONNECTS TO INTERCONNECT BOARD


NOTES:
H ECL High 4.2V
L ECL Low 3.6V
H TTL High ≥ 2.0V
L TTL Low ≤ .8V
AC
DC
FAST COUNTING DECADE
TIME BASE STEERING LOGIC
MULTIPLIER/TIME BASE SWITCHING
MULTIPLIER/TIME BASE GATING
MULTIPLIER/TIME BASE DECADES
RECLOCKING LOGIC
M CLEAR
REMOTE
10 MHz
fb SYN
÷ 4


M CLEAR
UPDATE
PRINT
ARM
GATE
M CLEAR
MARKER
REF. OUT
10 MHz
CONTROL LOGIC
START
STOP
DISPLAY TIME
STORAGE
REAR PANEL
INTERCONNECT BD.
FOR REFERENCE ONLY
RESET R.S. FLIP FLOP
REMOTE RESET
RESET SWITCH
REMOTE HOLD
INT. REFERENCE CONDITIONING
INT. & EXT. REF. IN
INT. REF. OUT
EXT. REF. IN
REF. OSC.
START/STOP
START/STOP LOGIC
EXT. GATE IN
START/STOP SWITCH
MODELS 8010B, 8030B
1 MHz
1 VOLT SWITCH
DISPLAY TIME ASSY. ON FRONT PANEL
PWR ON
OFF


Δt, M CLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
GATE
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
T2 CLEAR
UPDATE
f0/10
D1B
D1A
D1D
D1C
REF. OUT
10 MHz
PART OF J2
22
15
14
13
12
11
10
9
8
7
6
4
CC
AA
Z
T
S
P
N
M
L
K
J
H
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
18 VOLT SWITCH
FOR REFERENCE ONLY
DISPLAY TIME ASSY. ON FRONT PANEL
REF PART OF P2
CONNECT BD.
MC6 7400
MD6 7404
MD5 7402
MC5 74H00
ME2 7474 ARM CLR
ME3 3060 START CLR
ME3 3060 STOP CLR
MA0 7400
MA2 7404
Q9 2N4248
Q10 2N3646
Q19 2N3646
Q20 2N3646
Q21 2N3646
Q22 2N3646
Y1 9.9988 MHz
L1 22 μH
L2 2.2 μH
+5V
−18V
+18V


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 80108 AND 80208
P13 – USED ON MODELS 80208 AND 80308
SHADED COMPONENTS NOT USED ON MODEL 80208
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 8-32 x 5/8 SCREWS (61505B) AND LOCK WASHERS (61707B)
Y1 9.9988 MHz
SWITCH FAR SIDE
START/ STOP
RESET
MA5 7400
MA6 7400
MA7 7400
MA8 7454
MA9 7490
MA10 7490
MB8 7404
MB9 7490
MB10 7490
MC1 1010
MC2 7404
MC8 7454
MC9 7490
MC10 7490
MD1 1023
MD2 1034
MD3 1032
MD4 1027
MD8 7404
MD9 7490
MD10 7490
ME1 7474
ME2 7474
ME3 3060
ME4 7420
ME8 7420
ME9 7404
ME10 7490
MF3 7400
MF4 7400
MF5 7410
MF6 7400
MF7 7402
MF8 7454
MF9 7474
MF10 7400
A
B
C
D
E
F

PART OF J2

INT. & EXT. REF. IN — 25

GROUND — 21

+18V — 19

EXT. GATE IN — 17

$\overline{Fa}$ — 5

$\overline{Ck}$ — 3

REMOTE — 2

STORAGE — BB

GROUND — Y

+5V — X

−18V — W

$\overline{Fc}$ — V

REMOTE RESET — U

REMOTE HOLD — R

$\overline{TI}$ — F

$\overline{TIA}$ — E

$\overline{To}$ — D

$\overline{A/B}$ — C

$\overline{Pi}$ — B

$\overline{PA}$ — A

NOTE: UNLESS OTHERWISE SPECIFIED
ALL DIODES ARE 018
J2 CONNECTS TO INTERCONNECT BOARD

E4 fc
E3
E2
fa
E1

+5V C1 .01
MD1 1023
C2 20 pF
+18V R9 2.2K
CR1 CR2
R10 620
R8 470
R19 1.1K
R7 100
C3 .01
$\overline{A/B}$ $\overline{Ck}$ $\overline{Fa}$ MF5 7410

$\overline{Pi}$ $\overline{TI}$ ME6 7400
ME5 7400
ME5 7400
f/n
10 MHz
$\overline{PA}$ $\overline{Ck}$ MF5 7410
ME5 7400
COUNTER STEERING LOGIC

+5V R18 510
MD1 1023
R20 620
C6 3.3 pF
R21 620
R136 15K
R17 820

$\overline{TIA}$ R3 820
R14 510
Q23 2N3646

MD0 10131
C54 .01
R120 510
MD0 10131
MC1 1010
R118 510
R122 510

C55 .01
MD0 10131
MD0 10131
R121 510
R123 510
R119 510
R124 510
MC1 1010
R38 100
R47 1.8K
Q11 2N4258
R48 2.4K
C4 .01
R46 390
fb SYN

R15 510
R4 820
R34 4.7K
MC1 1010
R16 820
MC1 1010

MODELS 8010B, 8030B SYNCHRONIZER

E6 fb
E5

+5V C14 .01
MD2 1034
MD3 1032
MD3 1032
MD4 1027
C15 .01
$\overline{\Delta T}$
M CLEAR

R22 300
R24 100
R27 1.8K
R29 100
R31 24
R33 24
Q3 2N4258
Q4 2N4258
Q5 2N4258
Q6 2N4258
R23 390
R26 2.4K
C13 .01
R28 390
R30 75
R32 75
MC2 7404
MC5 74H00
MC2 7404
D_{1D}
$f_a/10$
D_{1C}
D_{1B}
D_{1A}
FAST COUNTING DECADE

Ck + Fa
$f_a/10$

$\overline{To}$ $\overline{Fa}$ ME6 7400
ME8 7404
$\overline{Ck}$ $\overline{Pi}$ ME6 7400
ME7 7402
$\overline{Fc}$ $\overline{TI}$ MF7 7400
10 MHz
$\overline{A/B}$
fb SYN
MF8 7454
To
ME8 7404
+5V C56 10 µF
R5 20
fb
Q1 2N4258
R6 75
MF3 7400
f_{bT}
$\overline{TIA}$ MD8 7404
$\overline{Pa}$ MD8 7404
+5V R12 24
fa'
R11 100
Q2 2N4258
R13 75
ME5 7400
MF3 7400
f_{aT}
TIME BASE STEERING LOGIC
$\overline{Fc}$

MF9 7474
MF9 7474
MF10 7400
MF10 7400
MF7 7400
MF10 7400
MF10 7400
÷ 4
D_{00}
$\overline{T2}$ CLEAR
MB8 7404
MB8 7404
ME10 7490
Q_4 Q_1
R_9 R_0
C7 .001

REMOTE
R35 4.7K

NOTES:
- (H) ECL High 4.2V
- (L) ECL Low 3.6V
- [H] TTL High ≥ 2.0V
- [L] TTL Low ≤ .8V
- AC
- DC

NOTES:

(H) ECL High 4.2V

(L) ECL Low 3.6V

[H] TTL High ≥2.0V

[L] TTL Low ≤.8V

AC

DC

M CLEAR

FAST COUNTING DECADE

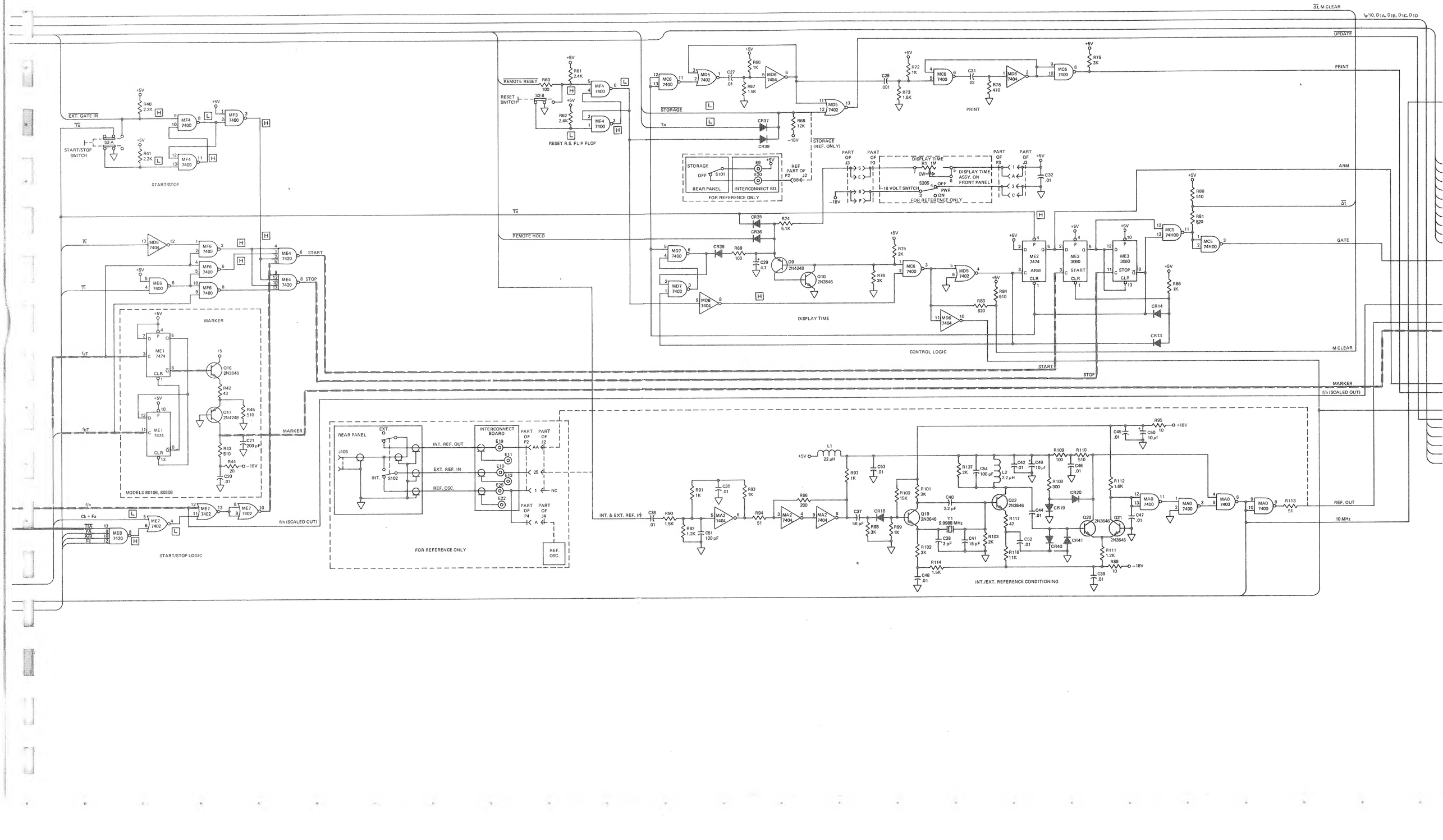
TIME BASE STEERING LOGIC

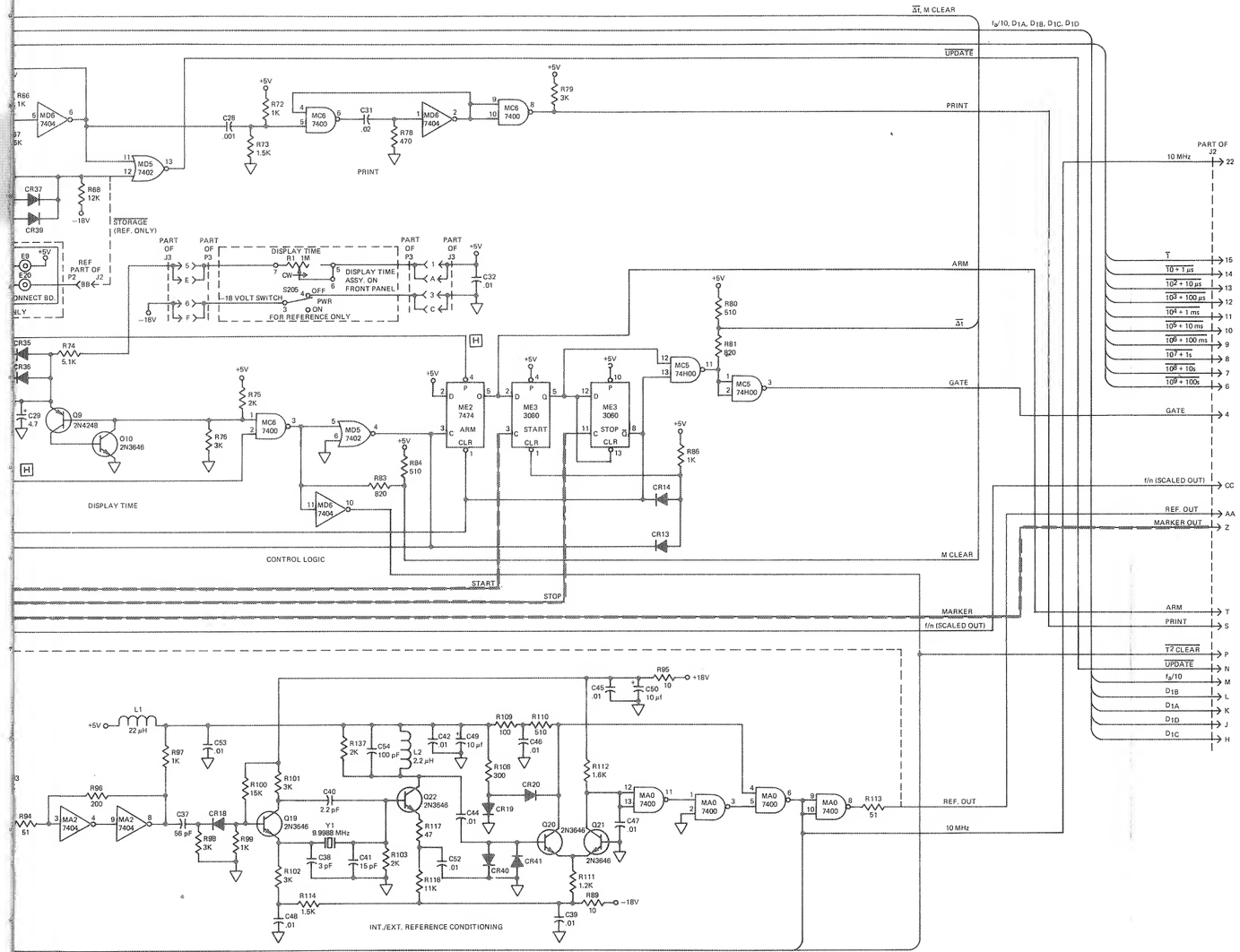
MULTIPLIER/TIME BASE SWITCHING

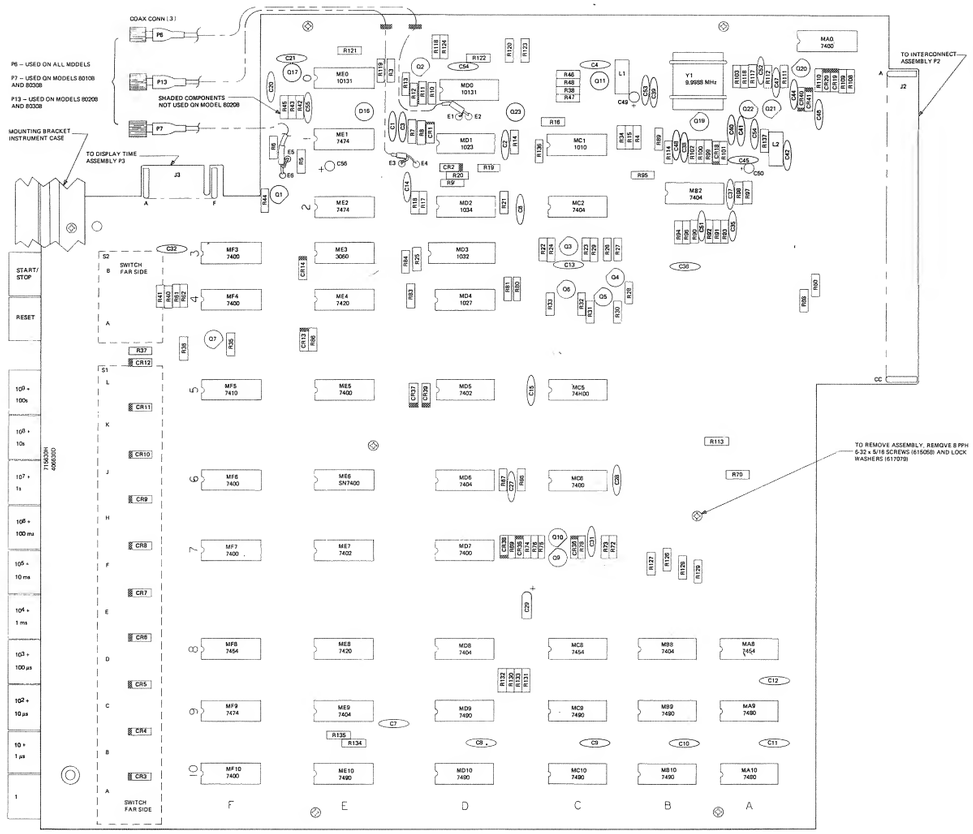
MULTIPLIER/TIME BASE GATING

RECLOCKING LOGIC

MULTIPLIER/TIME BASE DECADES


EXT. GATE IN
START/STOP SWITCH
START/STOP
REMOTE RESET
RESET SWITCH
RESET R.S. FLIP FLOP
REMOTE HOLD
STORAGE
STORAGE (REF. ONLY)
REAR PANEL
INTERCONNECT BD.
FOR REFERENCE ONLY
DISPLAY TIME
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
PWR ON
PRINT
CONTROL LOGIC
ARM
GATE
START
STOP
MARKER
MODELS 80108, 80308
START/STOP LOGIC
INT. REF. OUT
EXT. REF. IN
REF. OSC.
INT. & EXT. REF. IN
INT./EXT. REFERENCE CONDITIONING
REF. OUT
10 MHz
M CLEAR
UPDATE
f/n (SCALED OUT)


ΔT, M CLEAR
f0/10, D1A, D1B, D1C, D1D
UPDATE
PRINT
ARM
ΔT
GATE
GATE
f/n (SCALED OUT)
REF. OUT
MARKER OUT
M CLEAR
START
STOP
MARKER
f/n (SCALED OUT)
ARM
PRINT
T2 CLEAR
UPDATE
f0/10
D1B
D1A
D1D
D1C
10 MHz
T
10 + 1 µs
10² + 10 µs
10³ + 100 µs
10⁴ + 1 ms
10⁵ + 10 ms
10⁶ + 100 ms
10⁷ + 1s
10⁸ + 10s
10⁹ + 100s
PART OF J2
22
15
14
13
12
11
10
9
8
7
6
4
CC
AA
Z
T
S
P
N
M
L
K
J
H
DISPLAY TIME
CONTROL LOGIC
INT./EXT. REFERENCE CONDITIONING
STORAGE (REF. ONLY)
REF PART OF P2
DISPLAY TIME ASSY. ON FRONT PANEL
18 VOLT SWITCH
PWR ON OFF
FOR REFERENCE ONLY
ME2 7474 ARM CLR
ME3 3060 START CLR
ME3 3060 STOP CLR
MC5 74H00
MC6 7400
MD5 7402
MD6 7404
MC5 7400
R66 1K
R72 1K
R73 1.5K
R78 470
R79 3K
R68 12K
R74 5.1K
R75 2K
R76 3K
R80 510
RB1 820
RB4 510
RB3 820
RB6 1K
R95 10
R97 1K
R137 2K
R101 3K
R100 15K
R86 200
R84 51
R99 1K
R98 3K
R102 3K
R114 1.5K
R109 100
R110 510
R108 300
R112 1.6K
R111 1.2K
R89 10
R113 51
C28 .001
C31 .02
C32 .01
C29 4.7
C53 .01
C54 100 pF
C42 .01
C49 10 µf
C46 .01
C45 .01
C50 10 µf
C40 2.2 pF
C44 .01
C47 .01
C38 3 pF
C41 15 pF
C52 .01
C48 .01
C39 .01
L1 22 µH
L2 2.2 µH
Y1 9.9888 MHz
Q9 2N4248
Q10 2N3646
Q19 2N3646
Q22 2N3646
Q20 2N3646
Q21 2N3646
CR37
CR39
CR35
CR36
CR18
CR19
CR20
CR14
CR13
CR40
CR41
+5V
-18V
+18V


COAX CONN (3)
P6 – USED ON ALL MODELS
P7 – USED ON MODELS 8010B AND 8030B
P13 – USED ON MODELS 8020B AND 8030B
SHADED COMPONENTS NOT USED ON MODEL 8020B
MOUNTING BRACKET INSTRUMENT CASE
TO DISPLAY TIME ASSEMBLY P3
TO INTERCONNECT ASSEMBLY P2
TO REMOVE ASSEMBLY, REMOVE 8 PPH 6-32 x 5/16 SCREWS (6150B) AND LOCK WASHERS (6170B)
SWITCH FAR SIDE
START/ STOP
RESET
10⁸ + 100s
10⁷ + 10s
10⁶ + 1s
10⁵ + 100 ms
10⁴ + 10 ms
10³ + 1 ms
10² + 100 µs
10 + 10 µs
1
MAD 7400
ME0 10131
MD0 10131
ME1 7474
MD1 1023
MC1 1010
ME2 7474
MD2 1034
MC2 7404
MB2 7404
MF3 7400
ME3 3060
MD3 1032
MF4 7400
ME4 7420
MD4 1027
MF5 7410
ME5 7400
MD5 7402
MC5 74H00
MF6 7400
ME6 SN7400
MD6 7404
MC6 7400
MF7 7400
ME7 7402
MD7 7400
MF8 7454
ME8 7420
MD8 7404
MC8 7454
MB8 7404
MA8 7454
MF9 7474
ME9 7404
MD9 7490
MC9 7490
MB9 7490
MA9 7490
MF10 7400
ME10 7490
MD10 7490
MC10 7490
MB10 7490
MA10 7490
Y1 9.9988 MHz
F
E
D
C
B
A